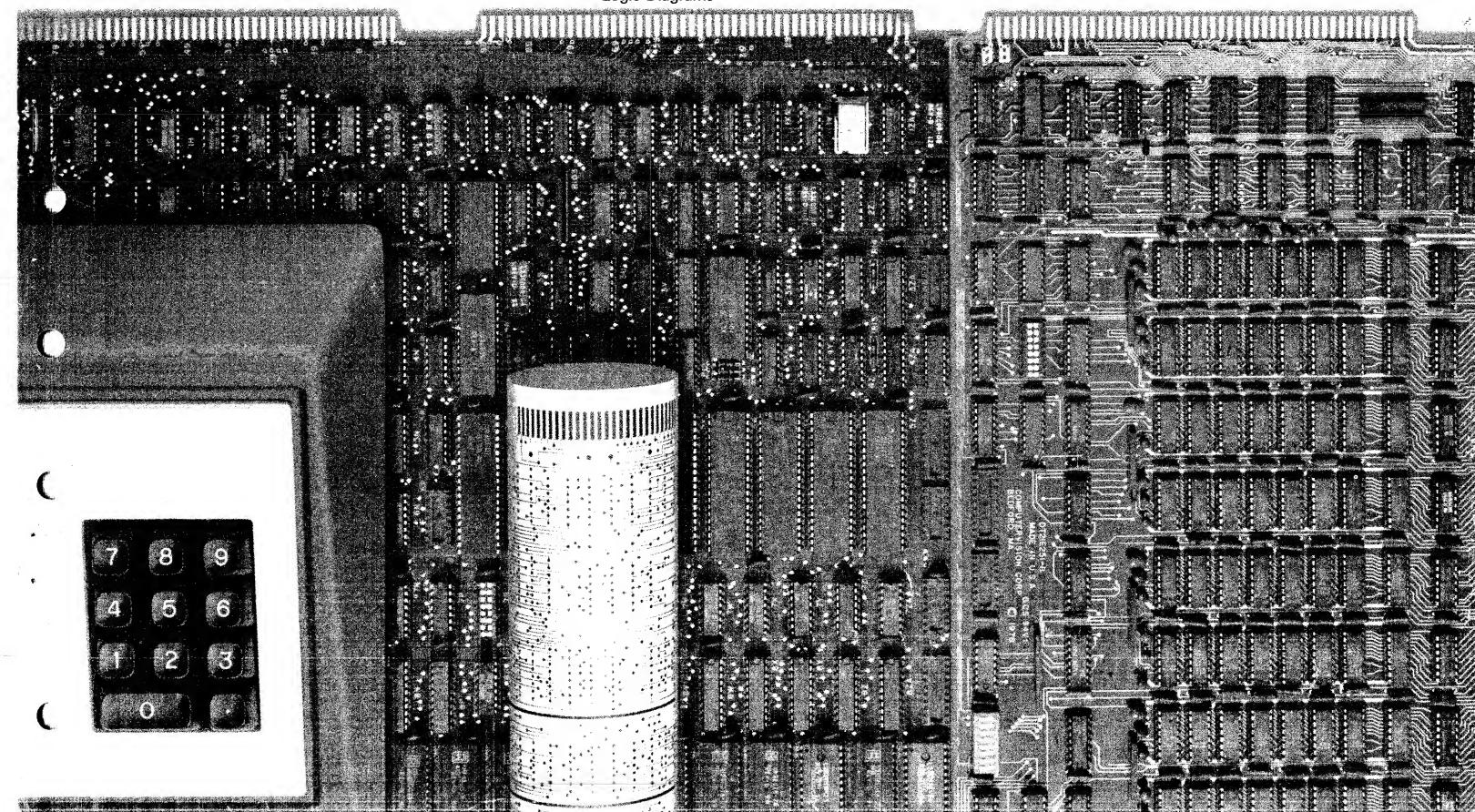


Technical

Computervision Graphics Processor (CGP) (CGP 80/180/100/200)

Logic Diagrams



Document control number:	73-00406
Name	

Computervision Graphics Processor (CGP) (CGP 80/180/100/200)

Logic Diagrams

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Logic diagrams pertain to:

- CGP 80*
- CGP 180*
- CGP 100 (A, B, and C)
- CGP 200 (A and B)
- CGP 200 (C)*

^{*}Also need EACPU/ICP Logic Diagrams

Table of Contents

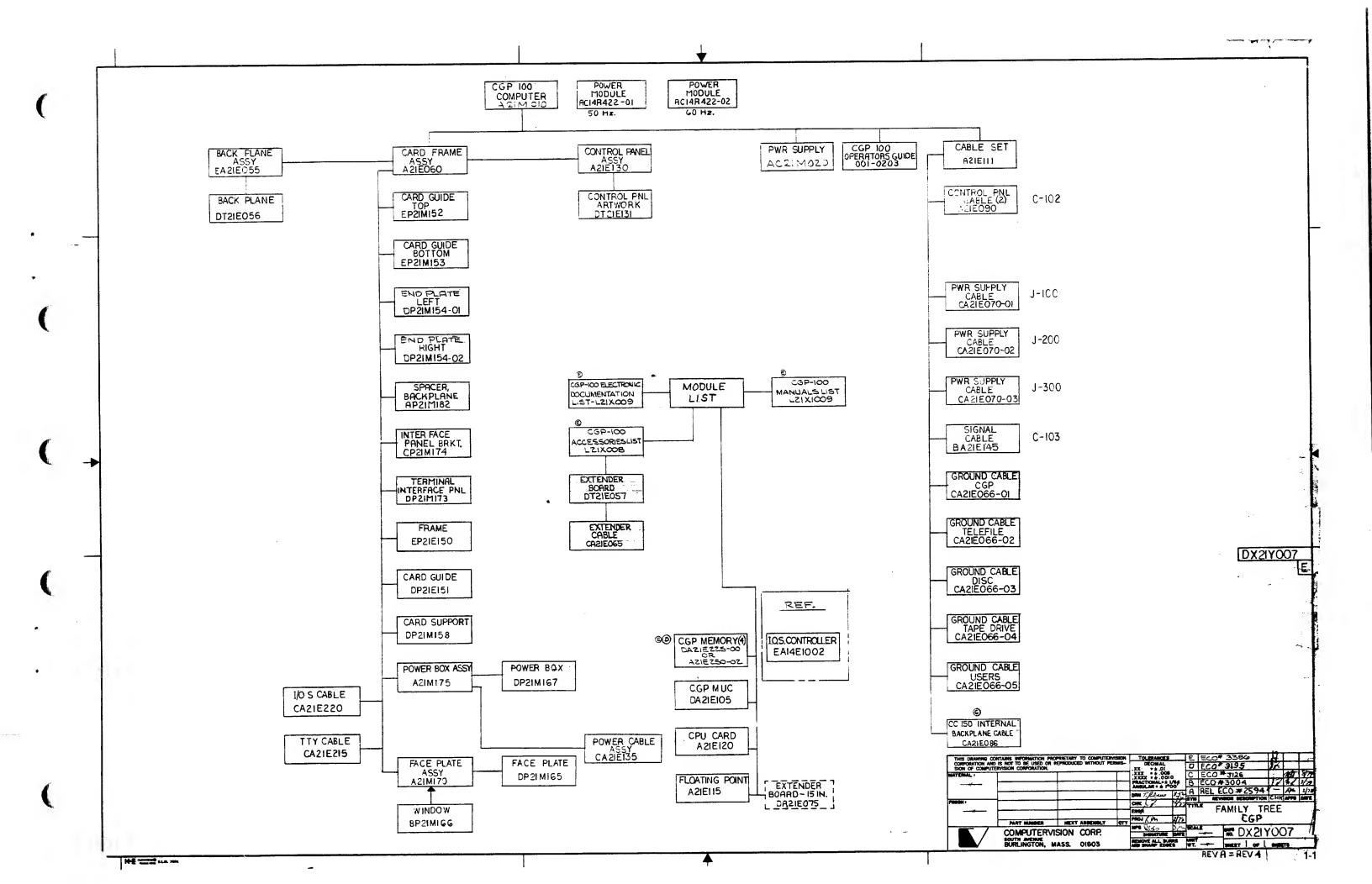
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4	Modules4-1Central Processor Unit (CPU) (Rev.L) DS21E1224-2Microprogram Flow Chart (Rev.E) DS21E0154-12Memory Management and Protection Unit (Rev.K) DS21E1074-40B-Port Management and Protection Unit (Rev.F) DS21E2824-45Floating Point Unit (FPU) (Rev.C) DS21E1174-50128K/32K A/B Port Memory Unit (Rev.G) DS21E2524-57Power Supplies4-73

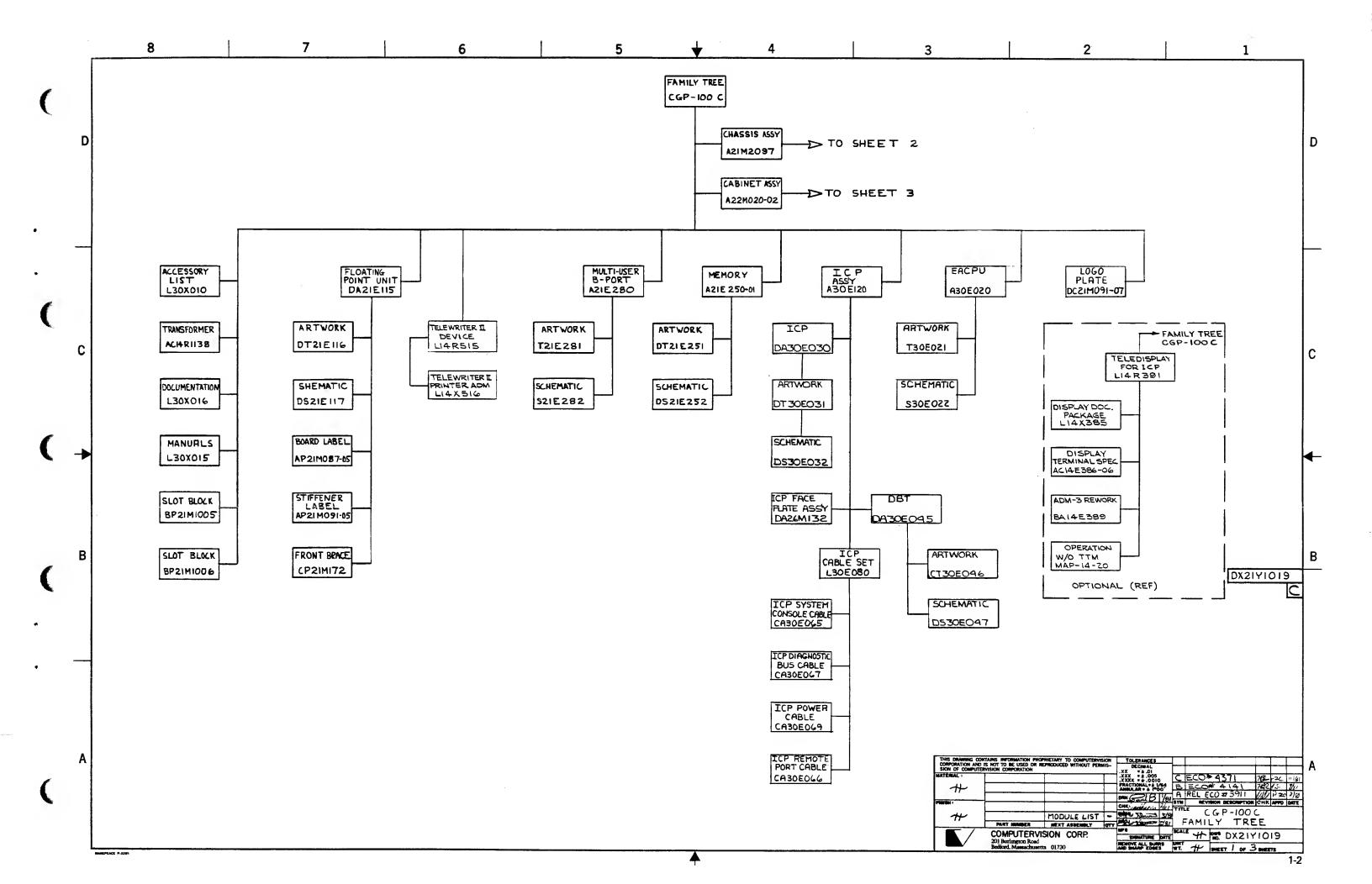
Introduction

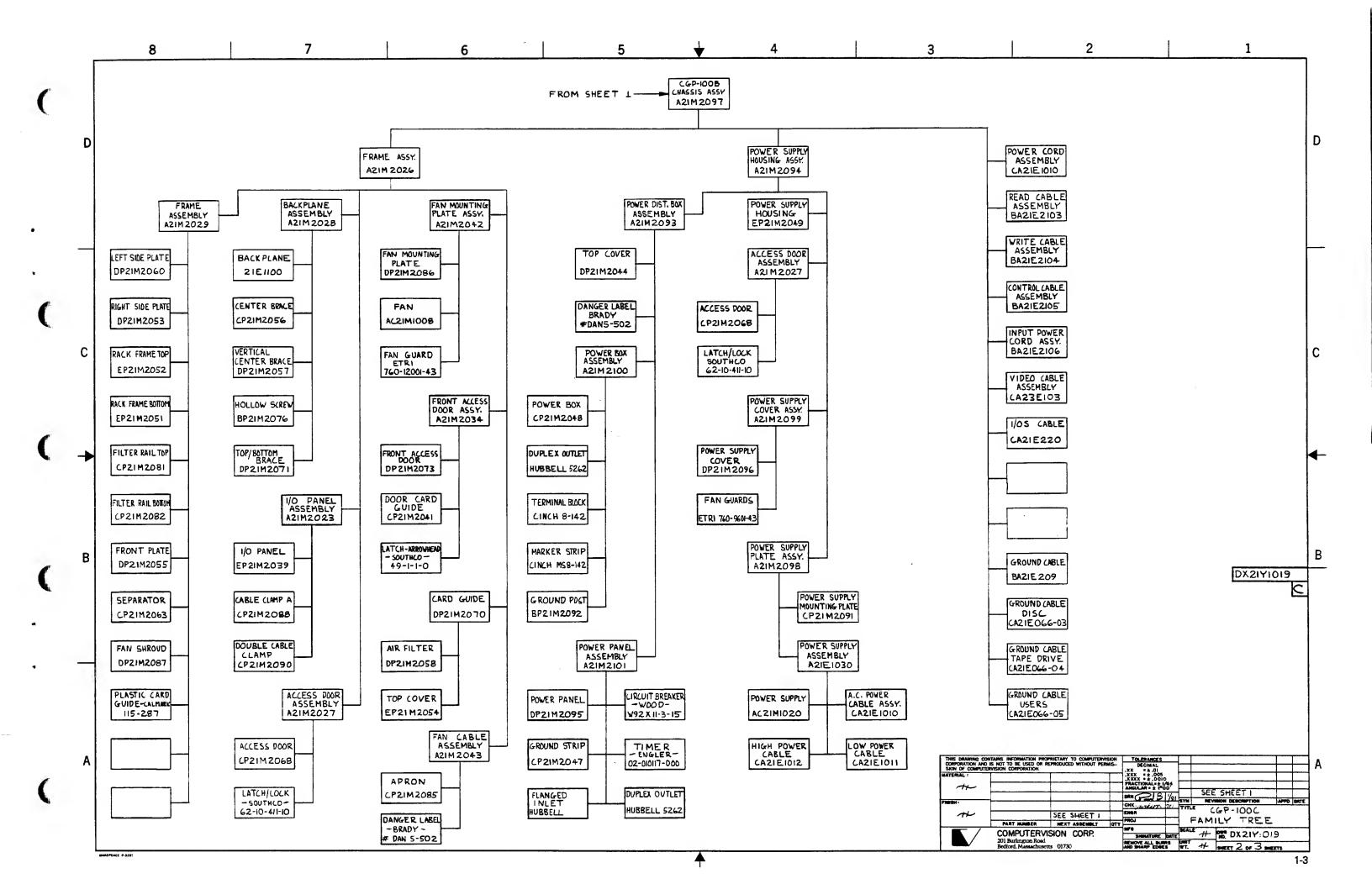
This manual contains the logic diagrams for the current models of the CGP line of Computervision Graphics Processors. This line includes the CGP-100 A, B. and C, CGP-180, and CGP-200 A, B, and C. To use this manual first determine which machine you are working on. Consult the family tree for a listing of boards that are part of that system. Next determine which boards (modules) you are interested in and then refer to the diagrams for the particular module. These are listed in the Table of Contents. The logic diagrams for the Extended Address Central Processing Unit (EACPU) and the Intelligent Control Panel (ICP) are shown in a separate publication "Extended Address Central Processing Unit (EACPU)/Intelligent Control Panel (ICP) Logic Diagrams". Order No. 001-00567.

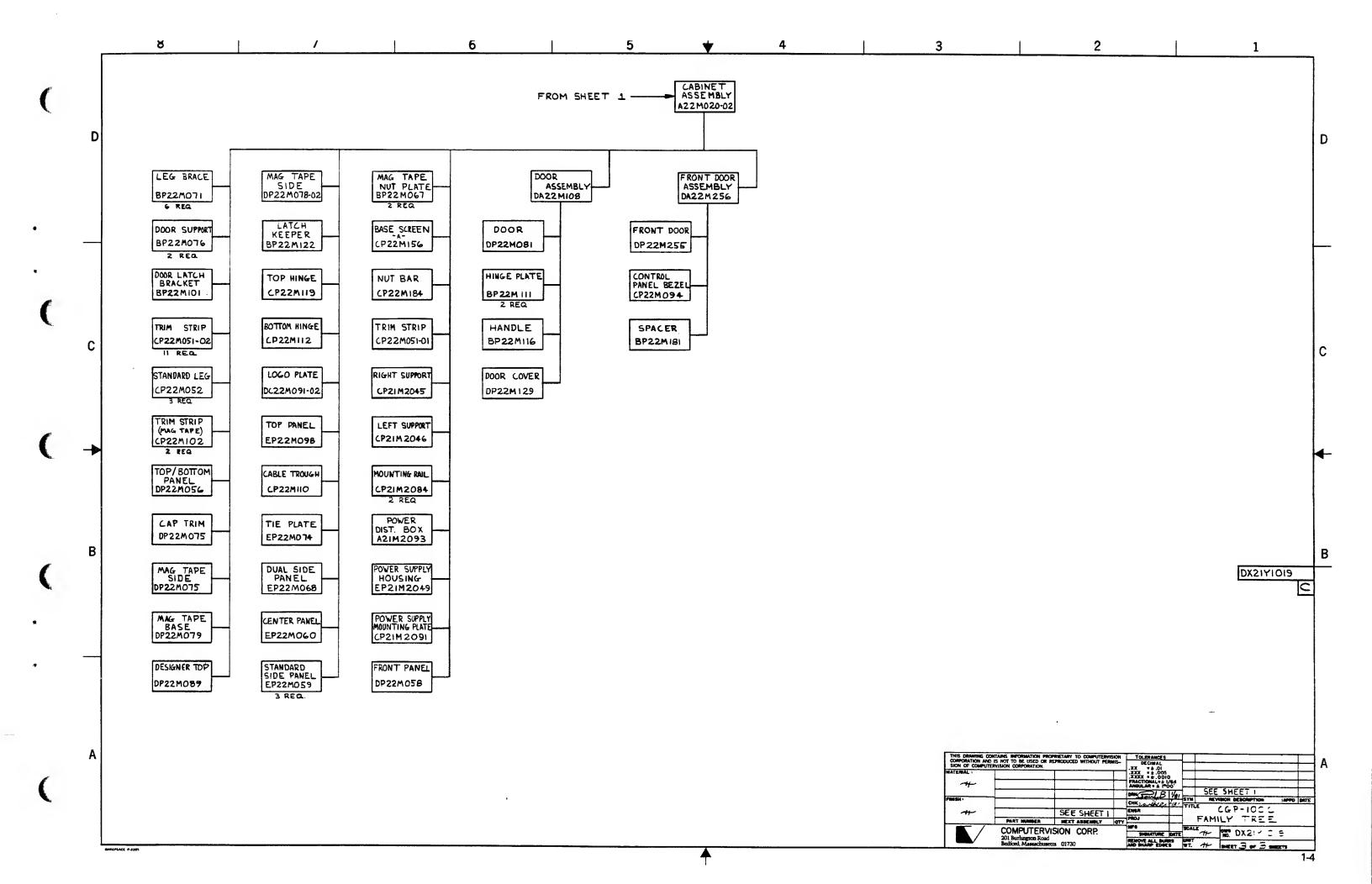
Section 1 Computervision Graphics Processors (CGP) Family Trees

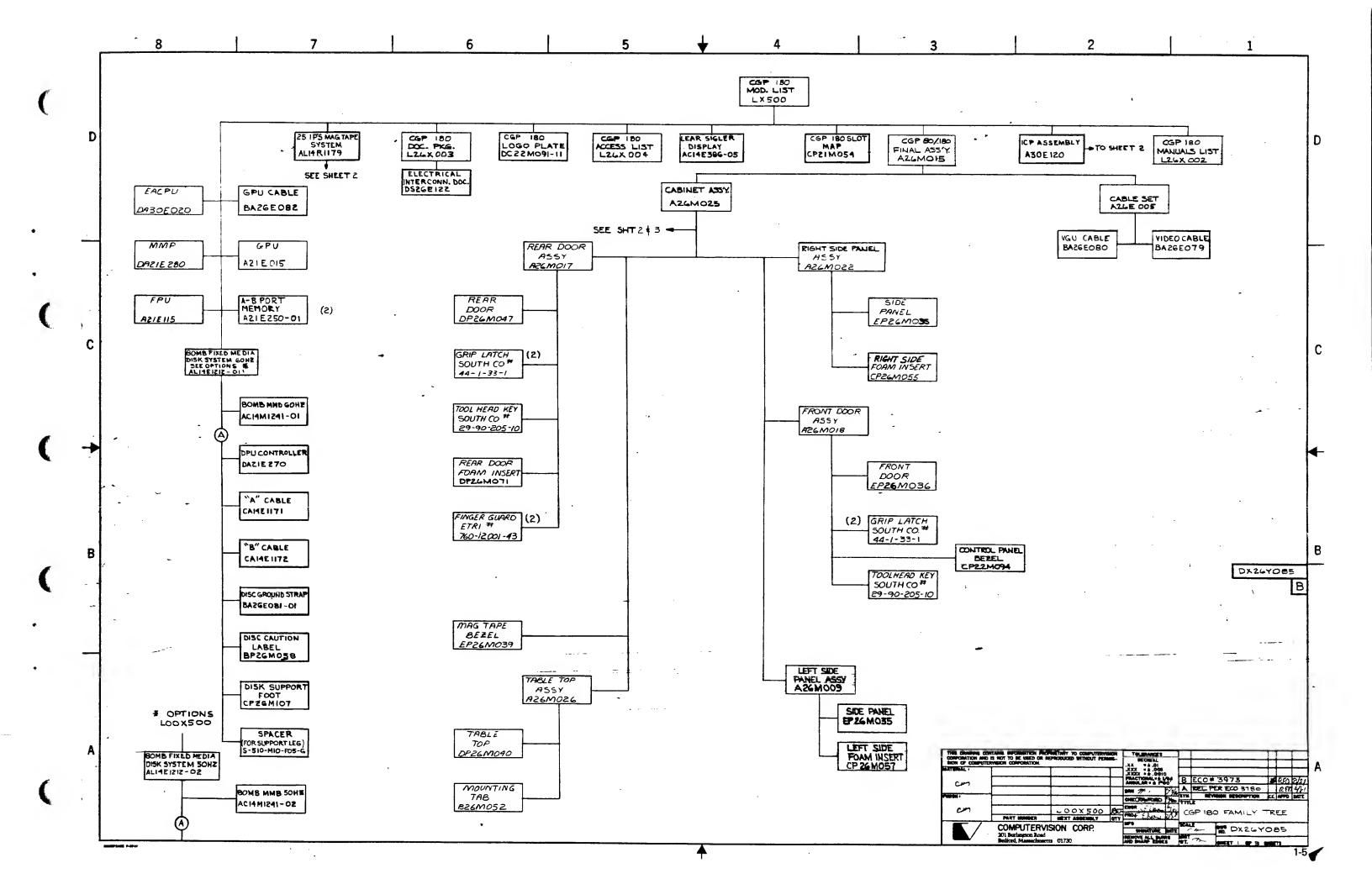
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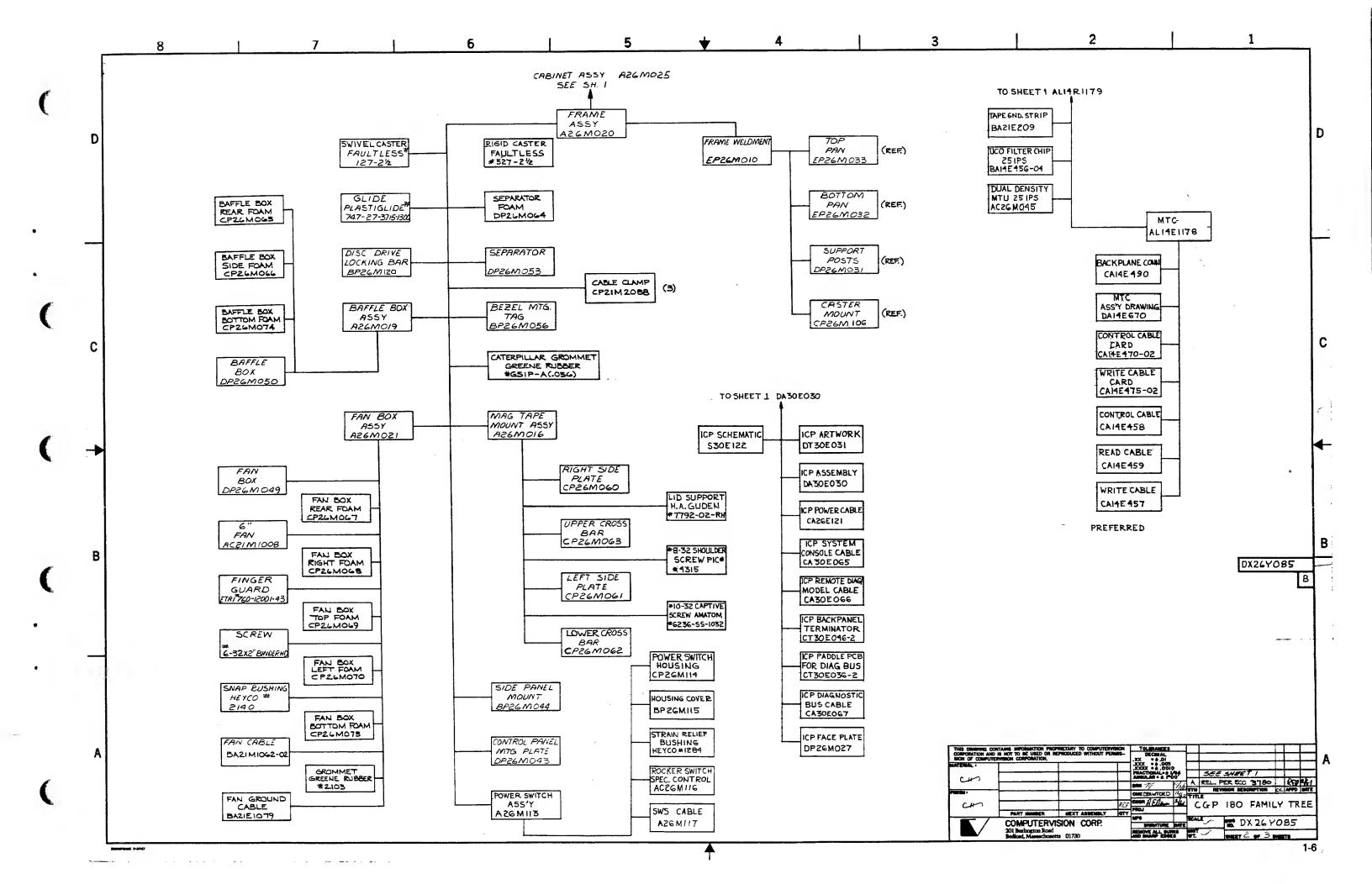


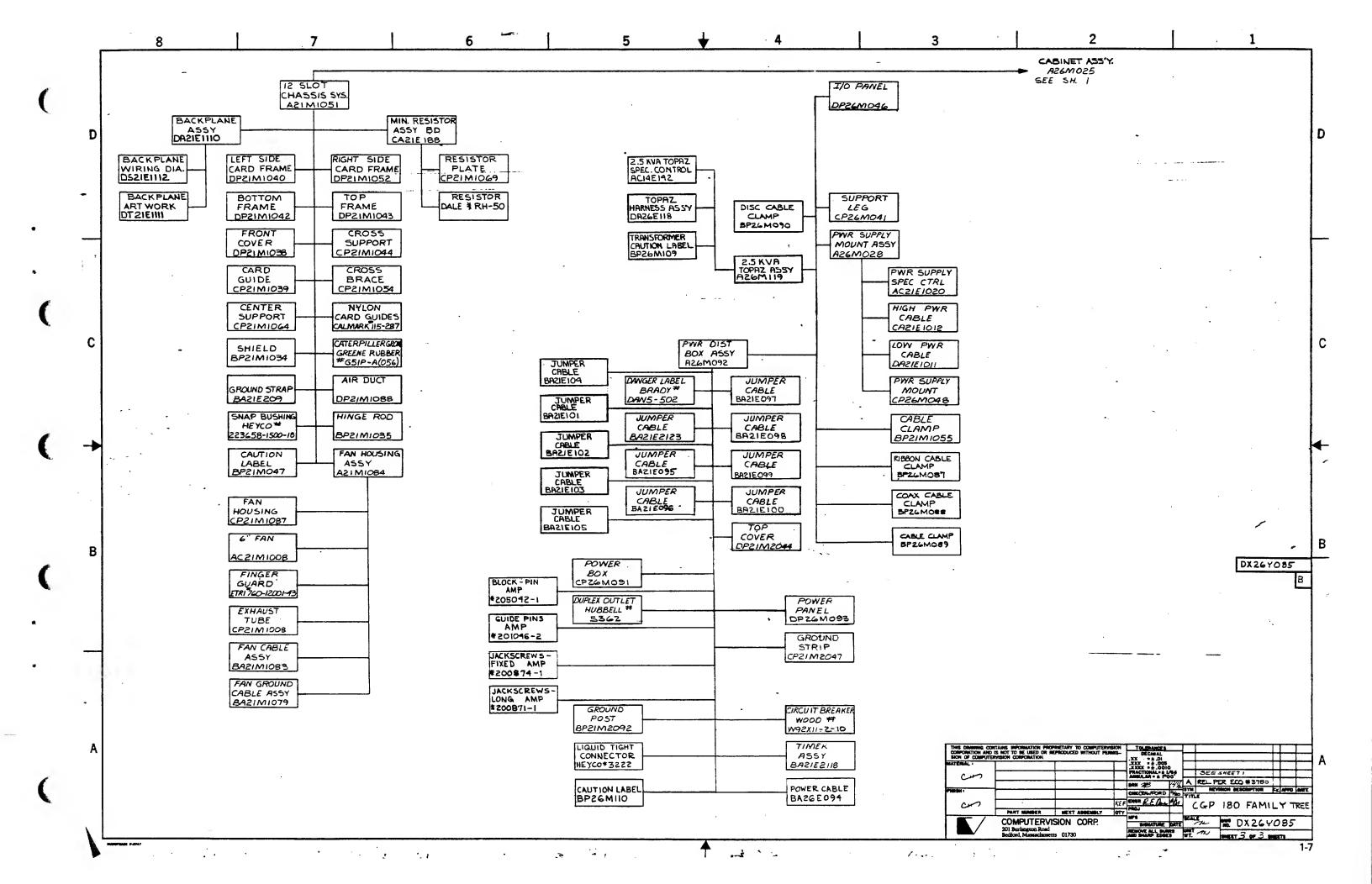


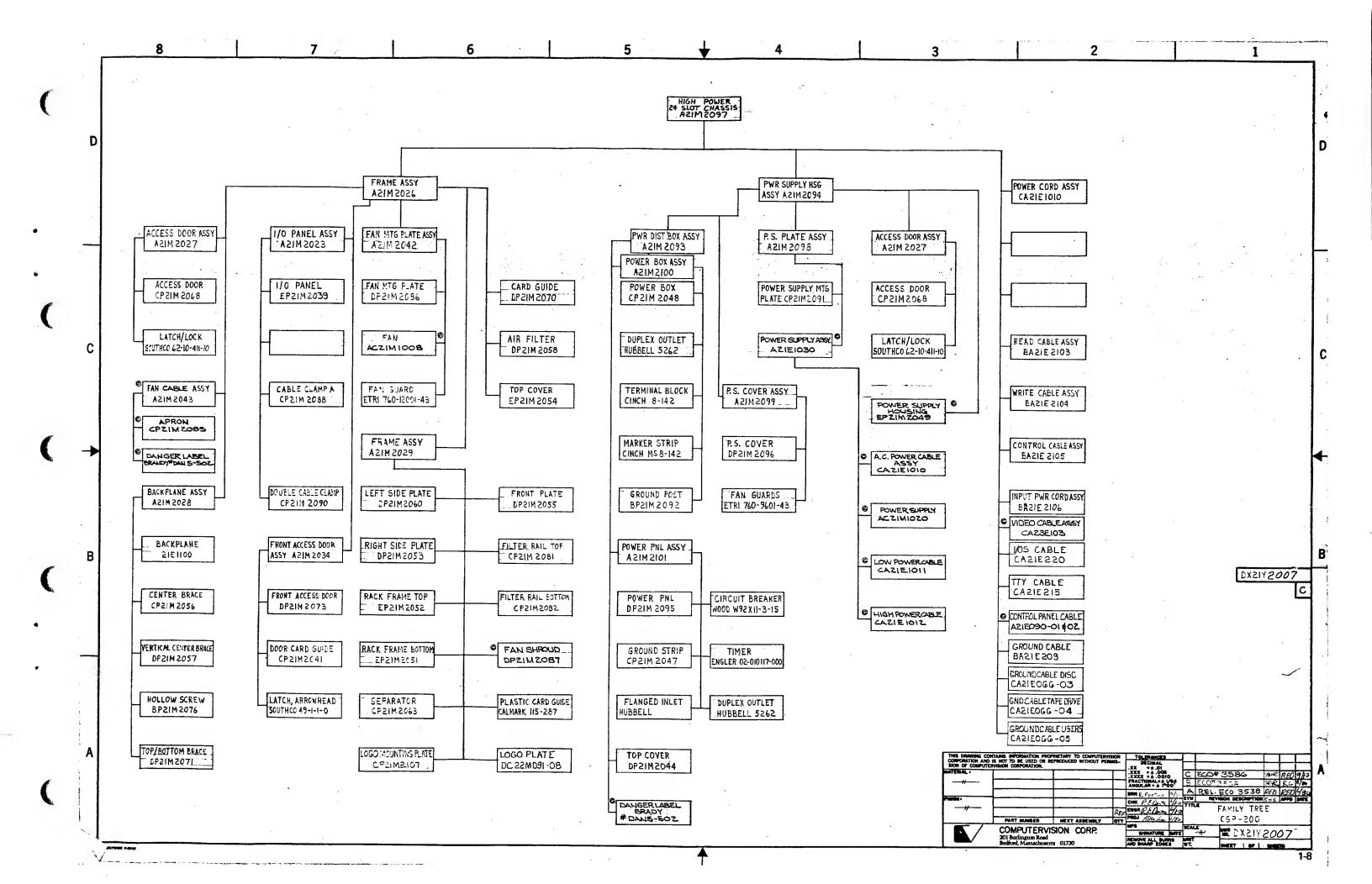


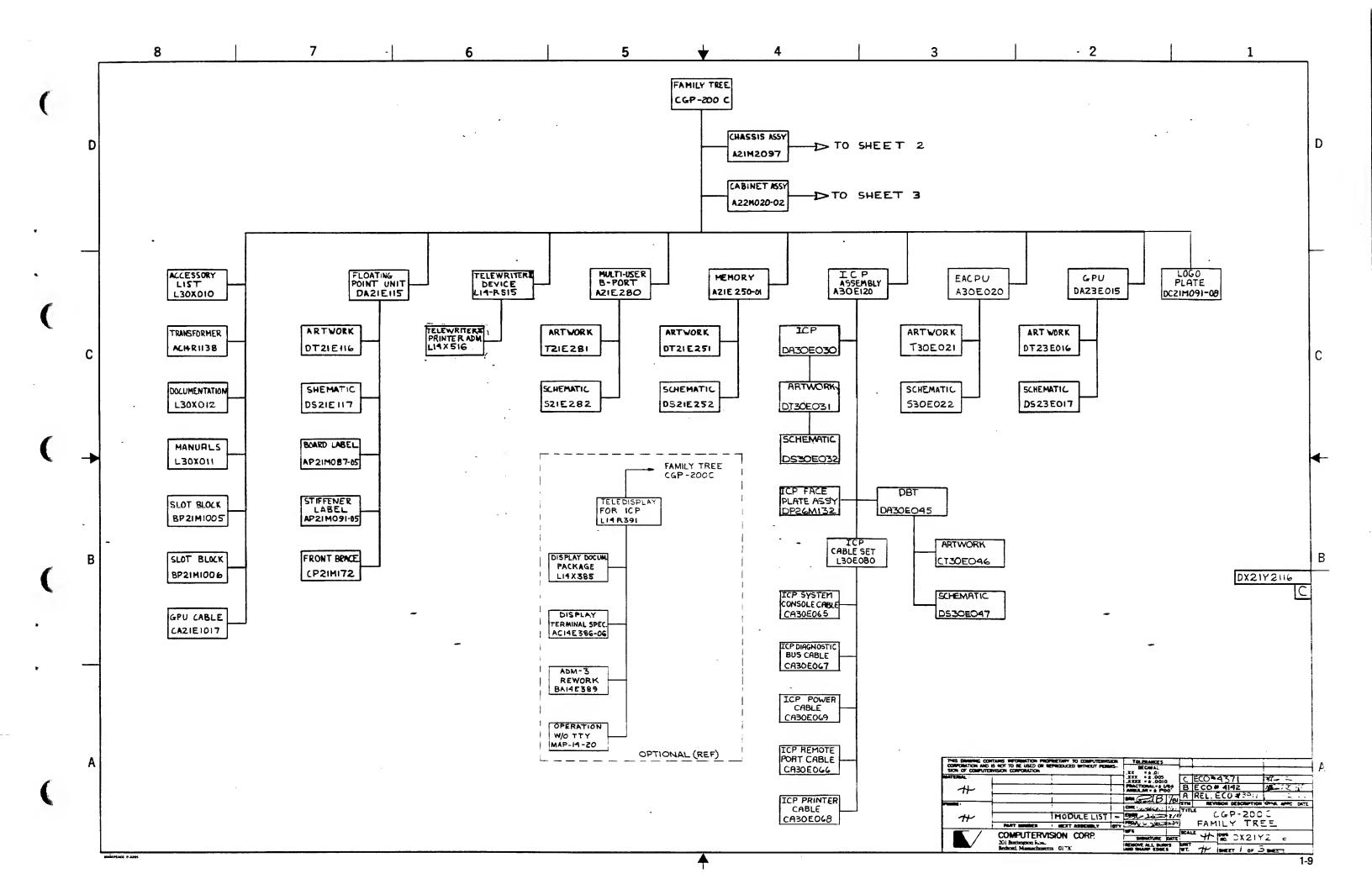


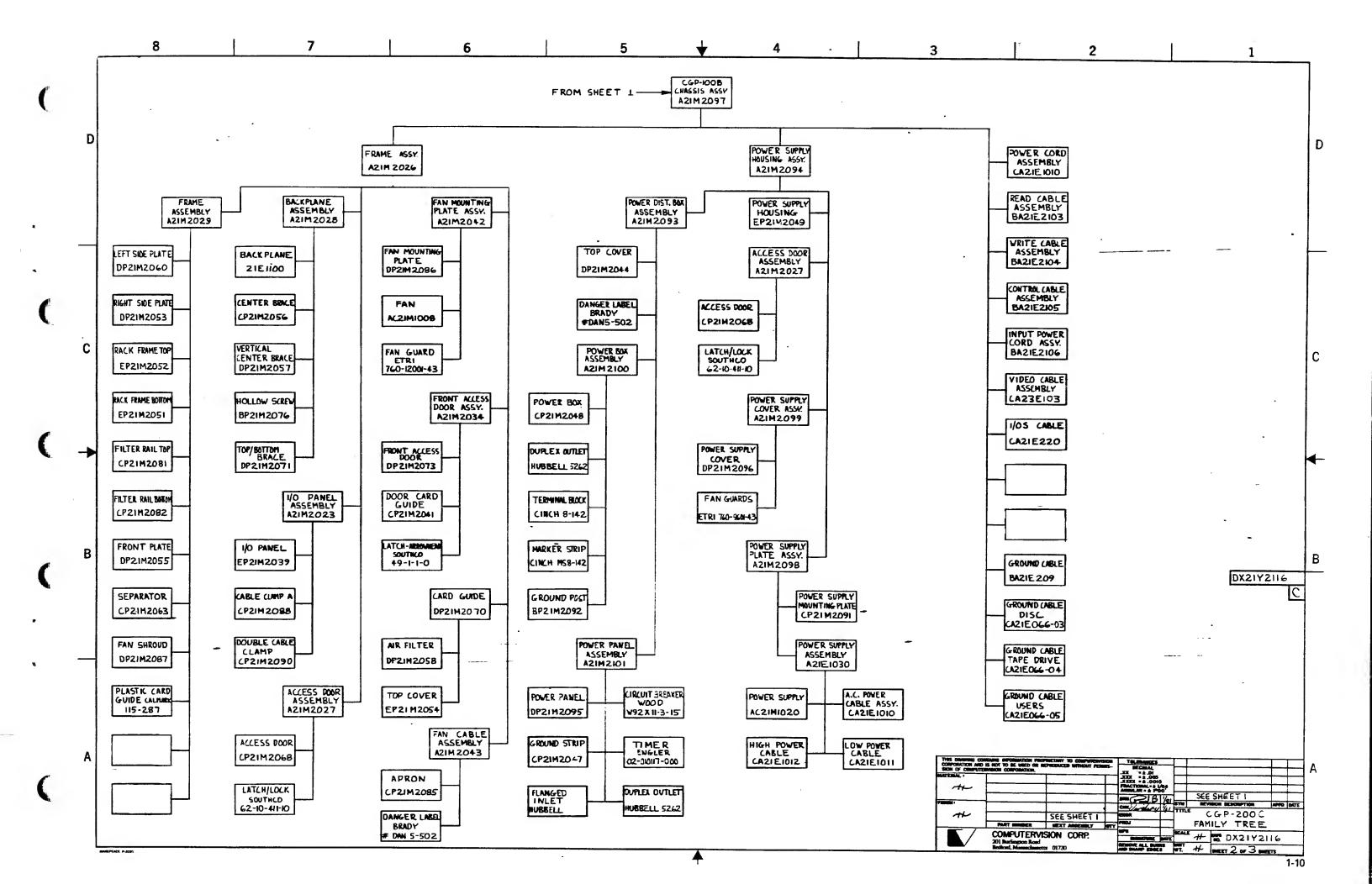


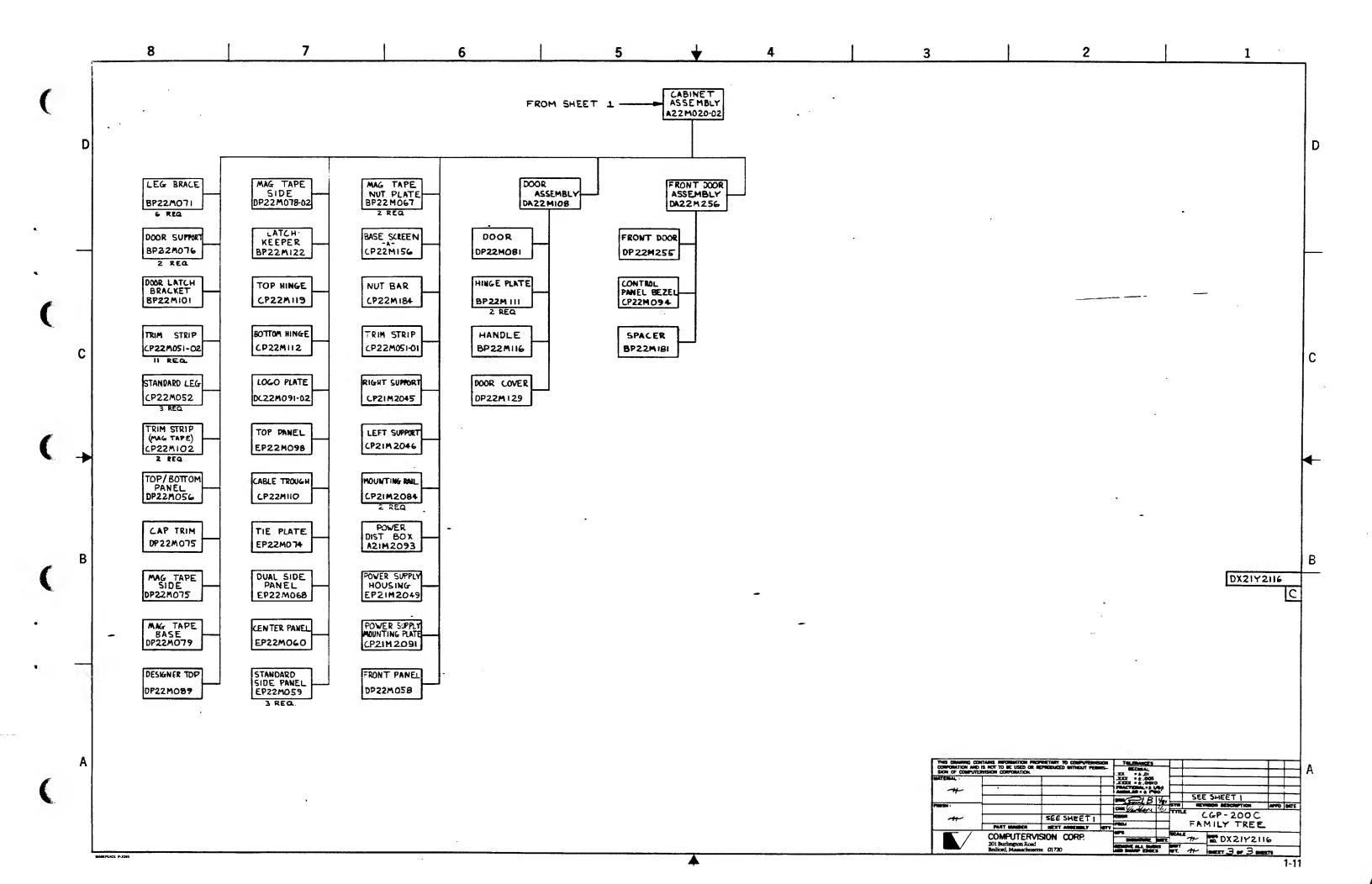






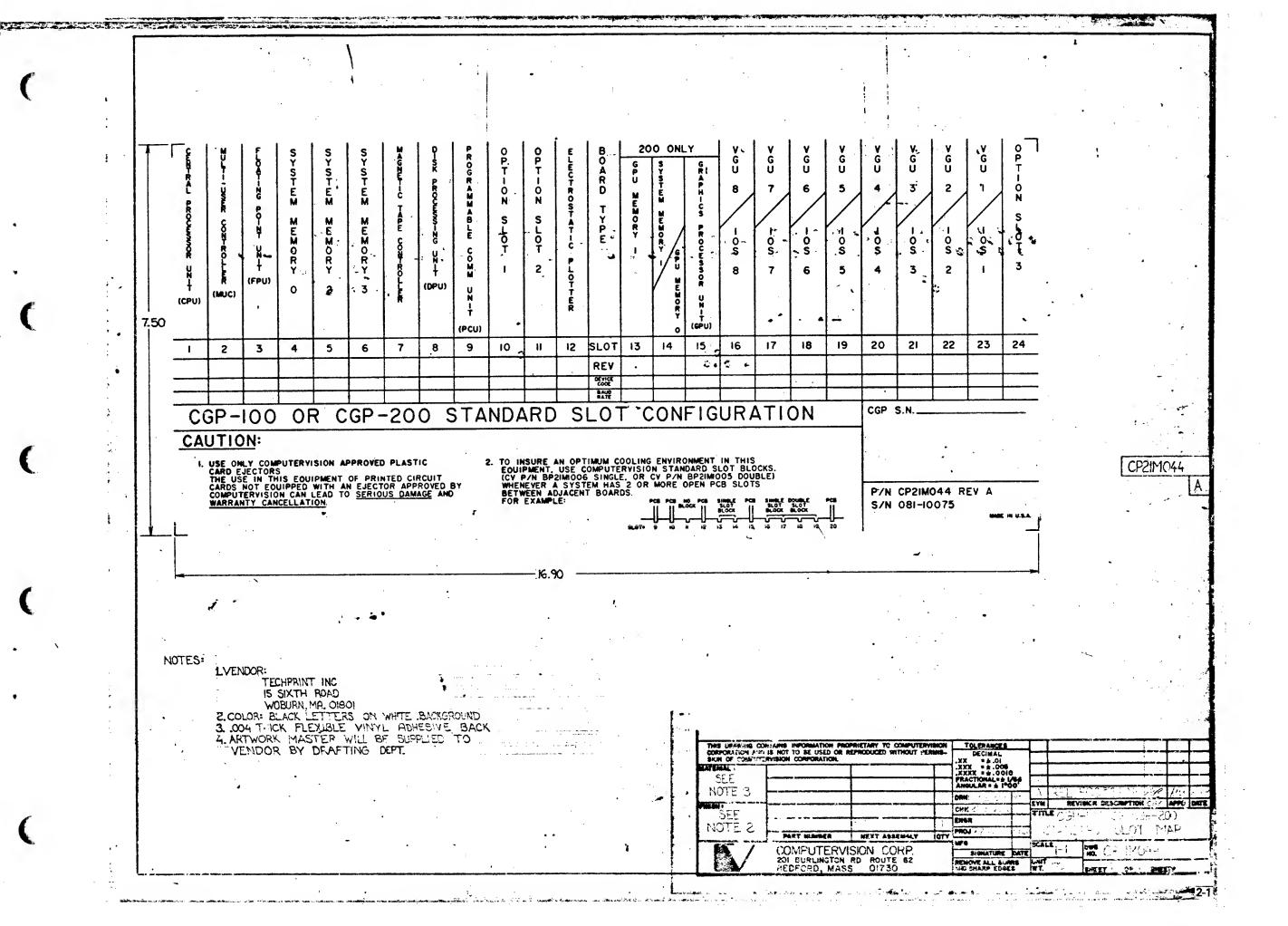


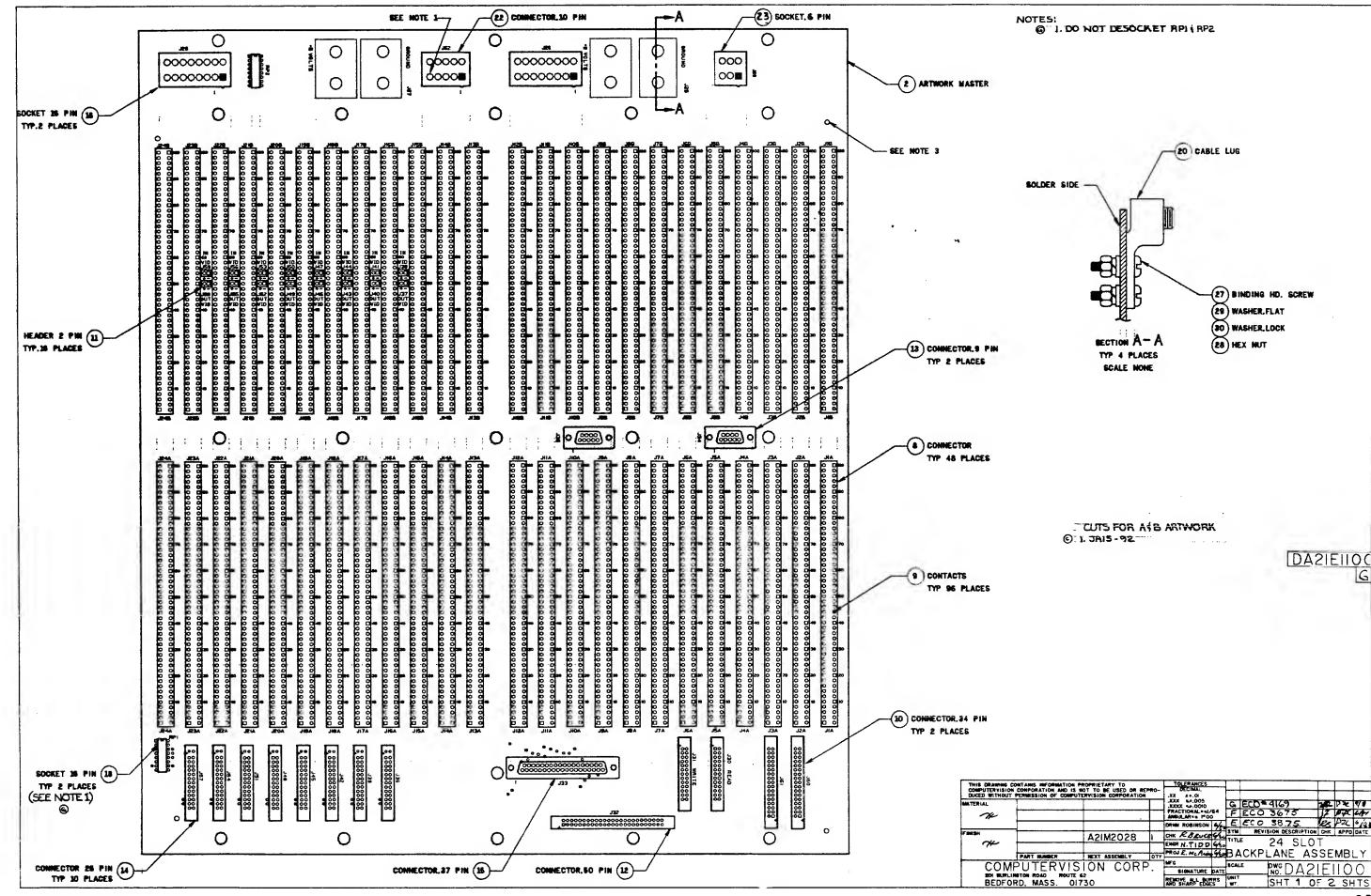


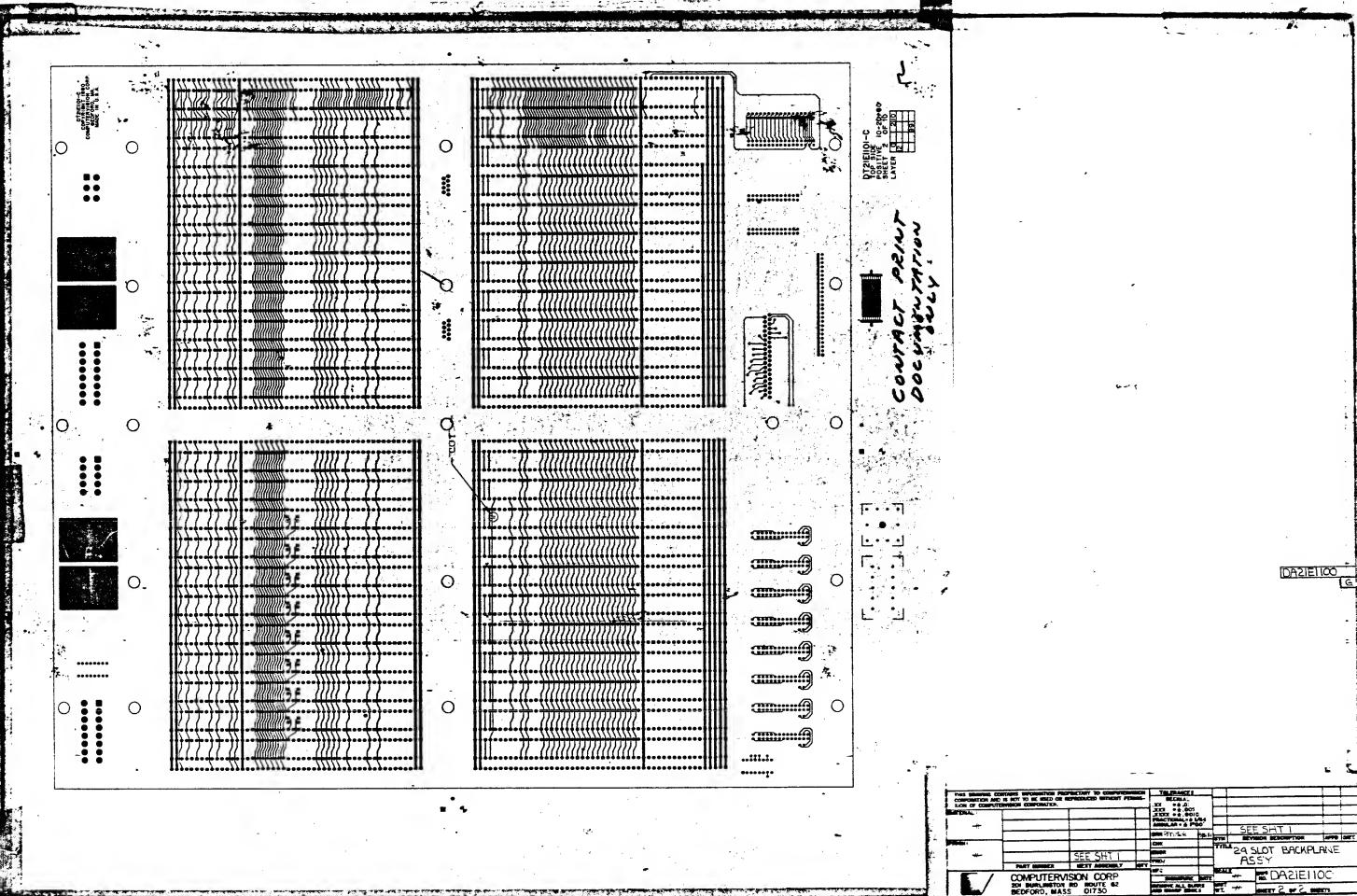


Section 2 Backplanes

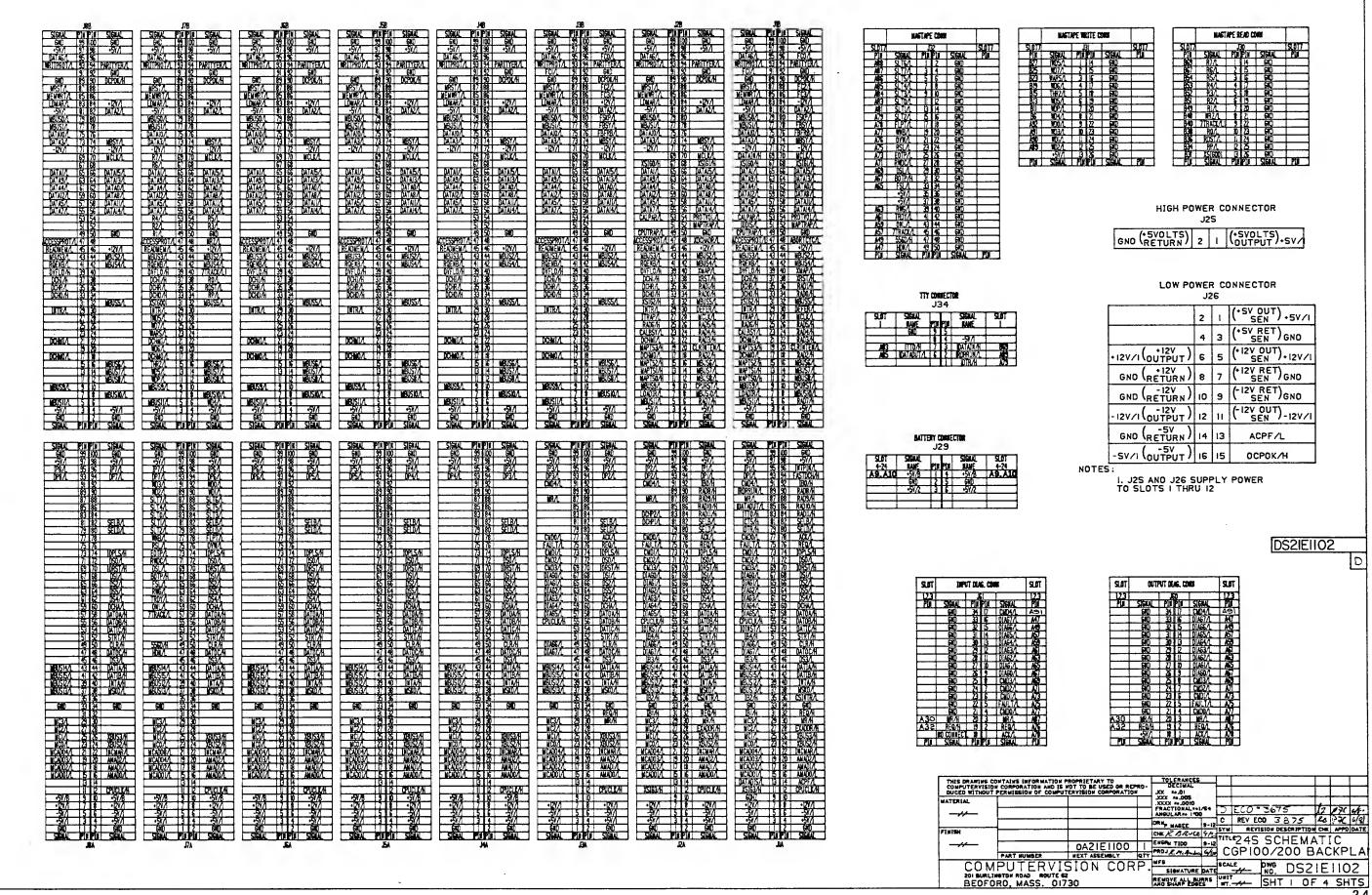
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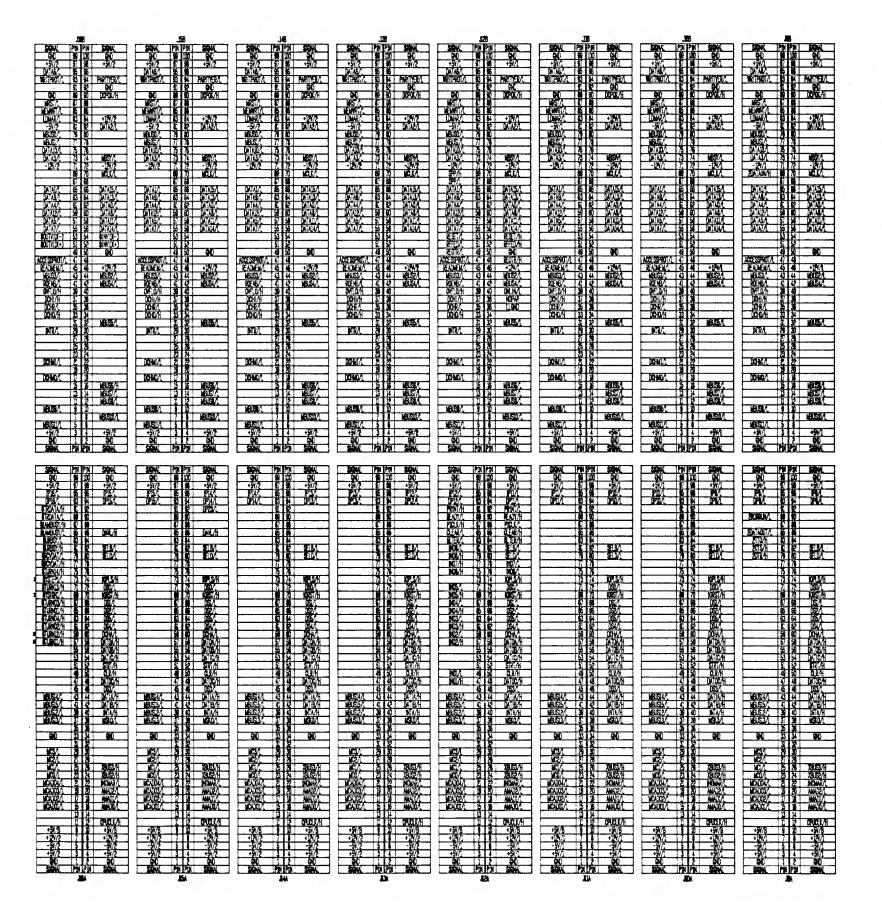


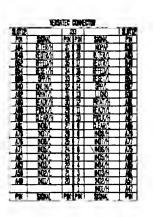


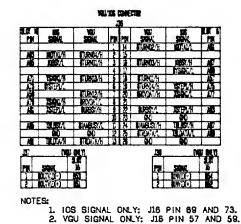


2-









THE PROPERTY J35

J82 +5V/2 2 1 +5V/2 GND 4 3 GND +12V/2 6 5 +12V/2 GND 8 7 GND -12V/2 10 8 DCPOK/H

HIGH POWER CONNECTOR GND (+5VOLTS) 2 1 (+5VOLTS) 5V/2

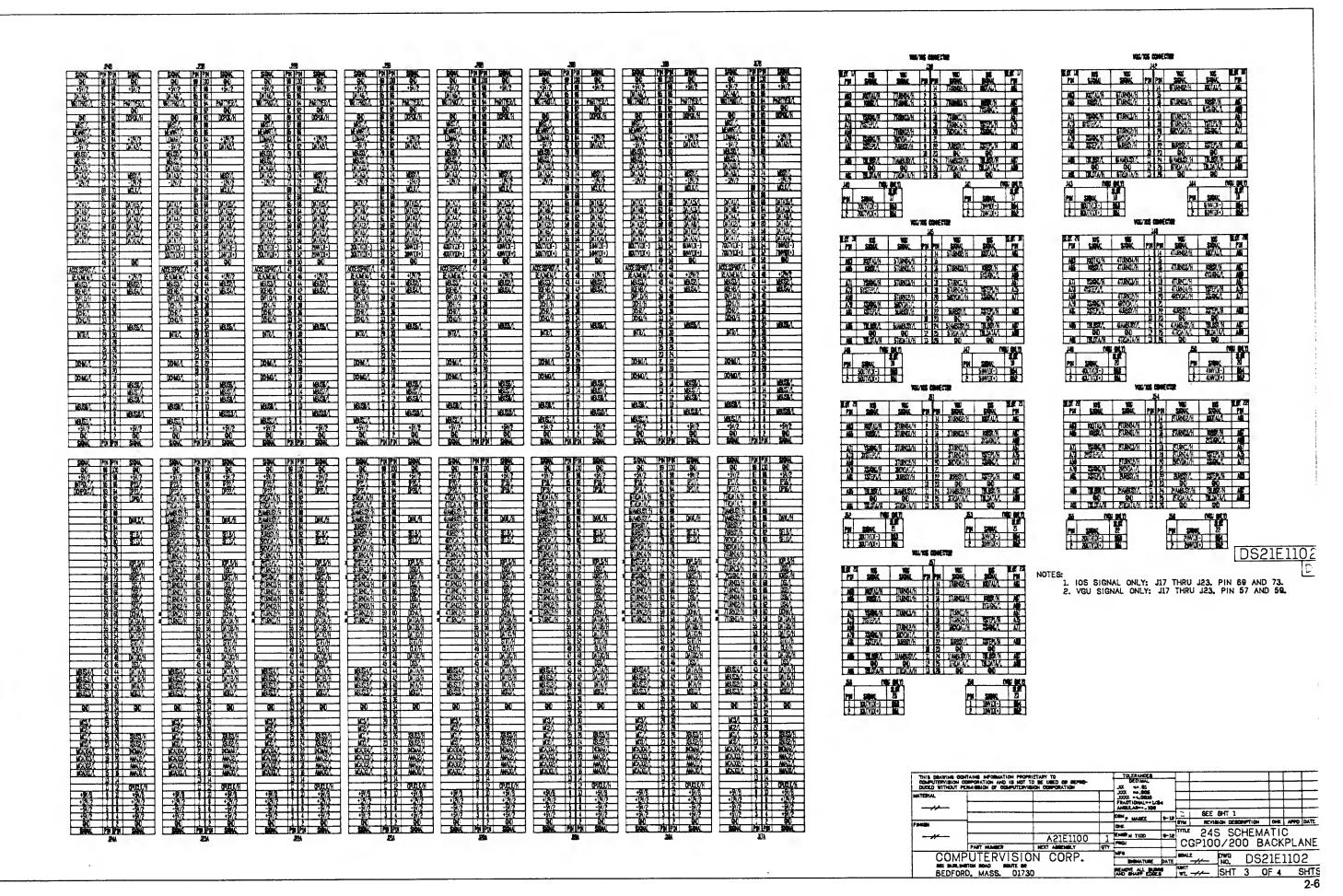
LOW POWER CONNECTOR

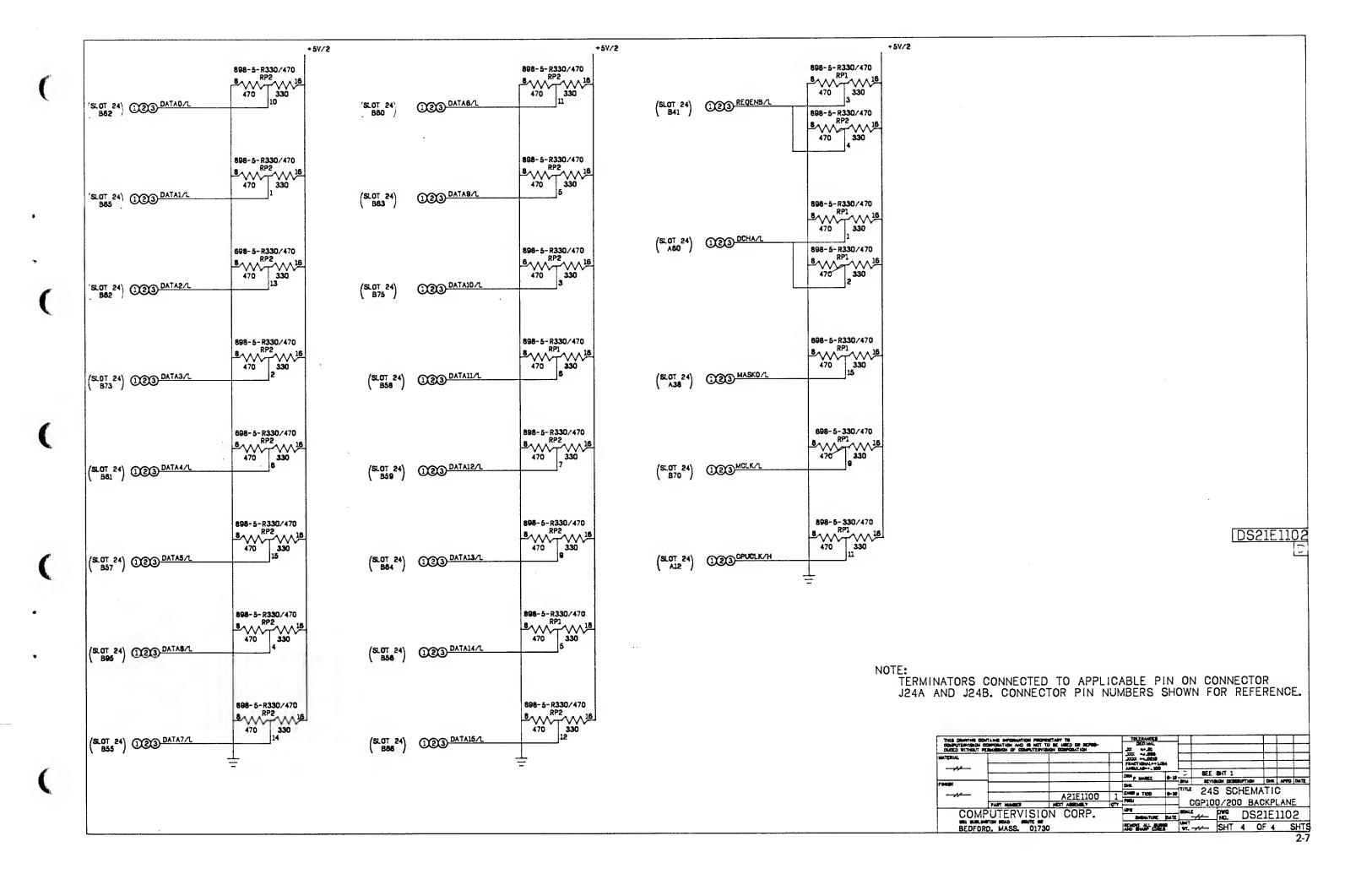
2 1 (+5V OUT)+5V/2 4 3 (+5V RET) GND +12V/2 OUTPUT) 6 5 (+12V OUT)+12V/2 GND (+12V) 8 7 (+12V RET) GND GND (-12V) 10 9 (-12V RET) GND -12V/2 OUTPUT) 12 11 (-12V OUT) 12V/2 GND (-5V) 14 13 ACPF/L -5V/2 (0UTPUT) 18 15 DCPOK/H

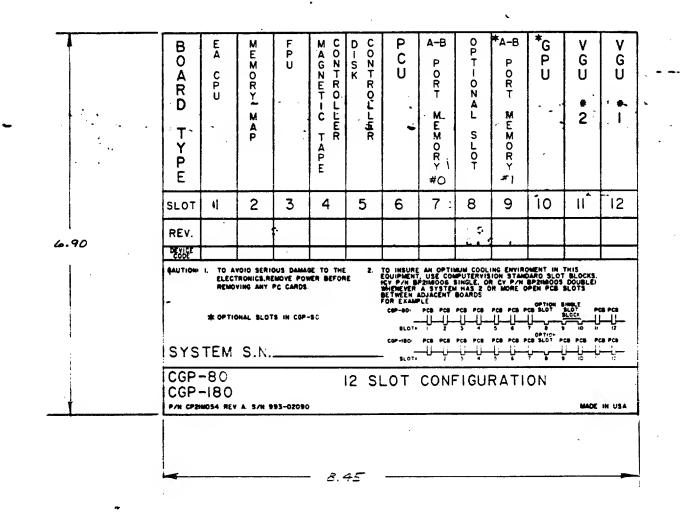
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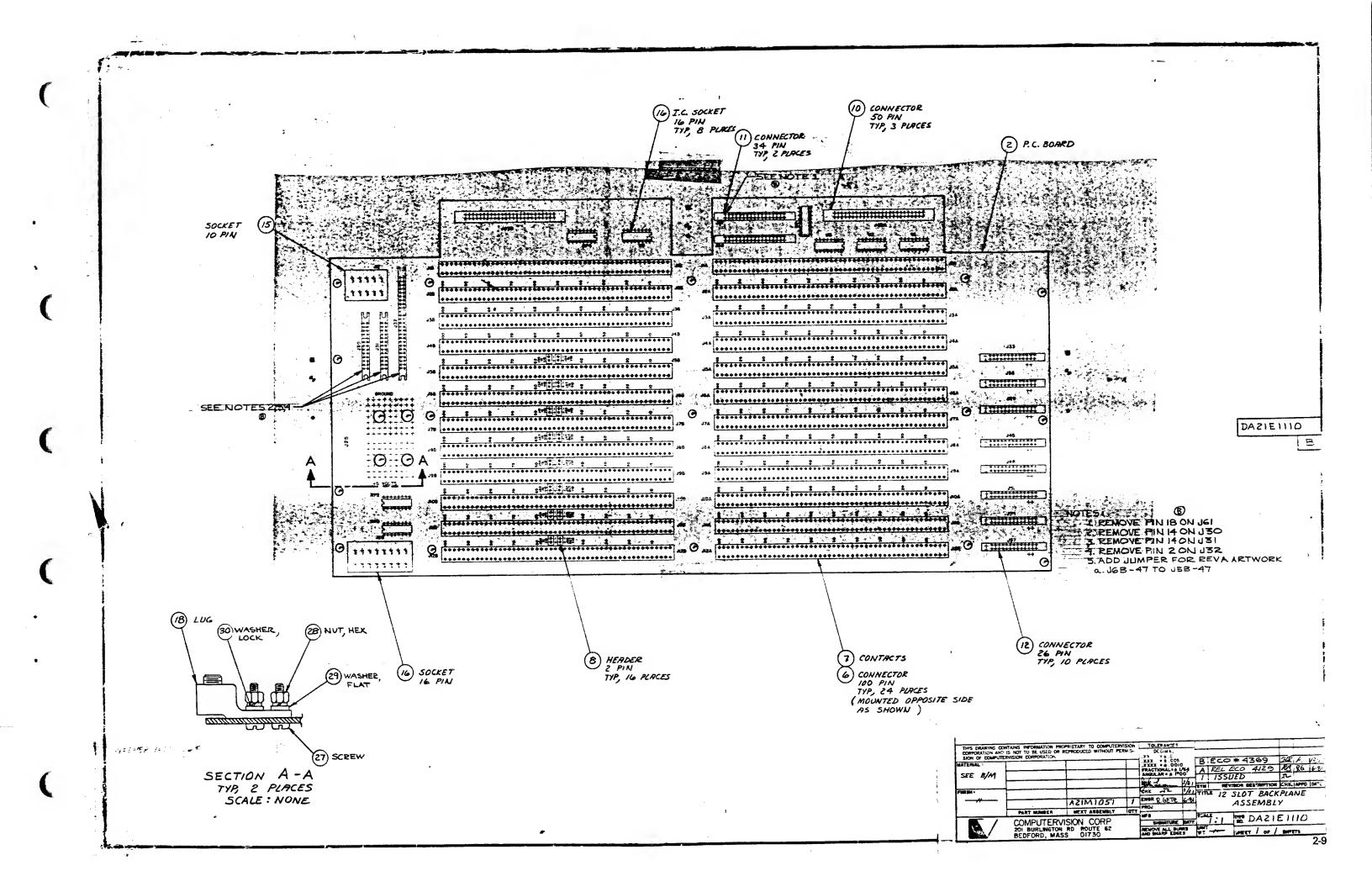


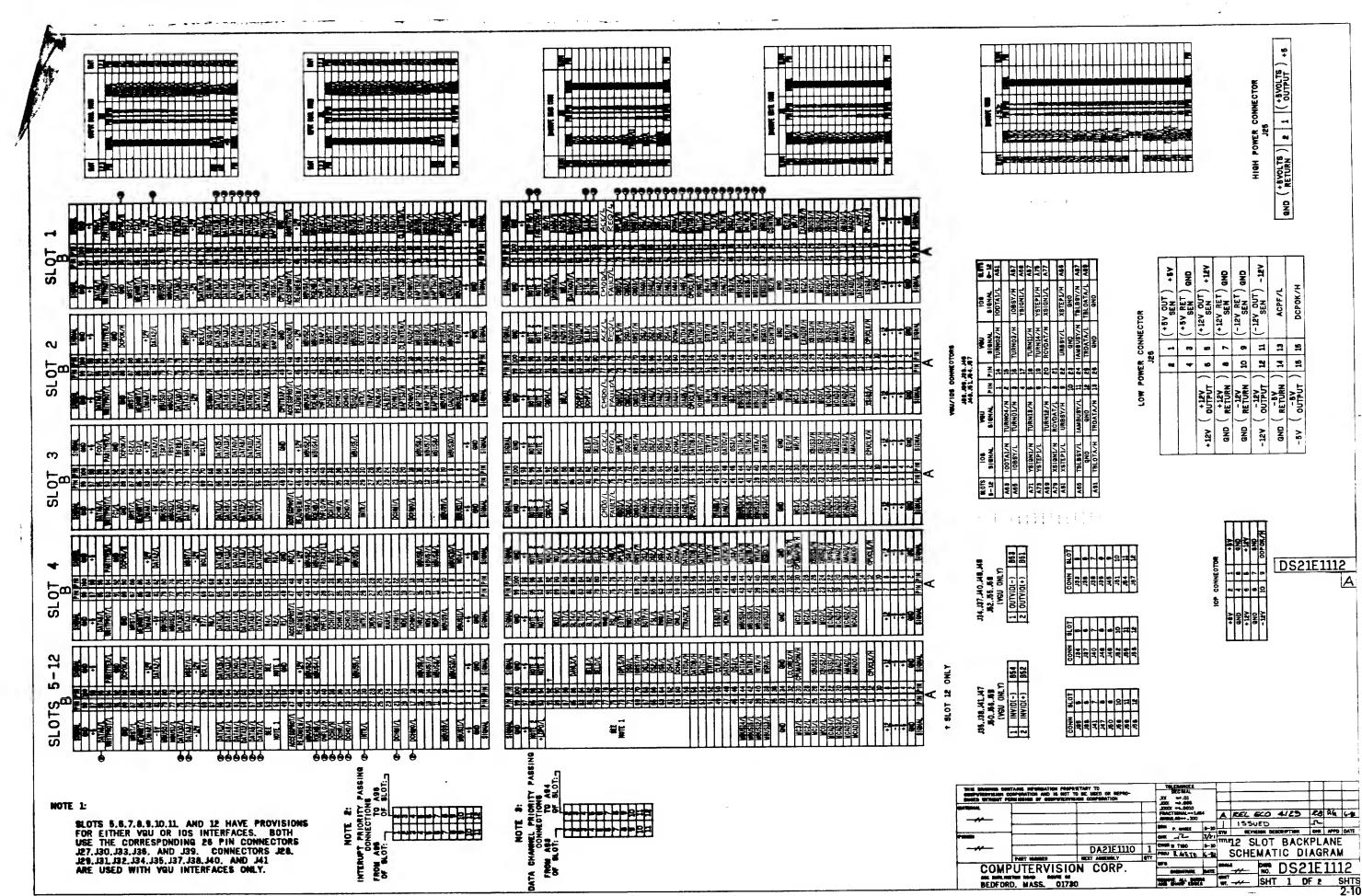
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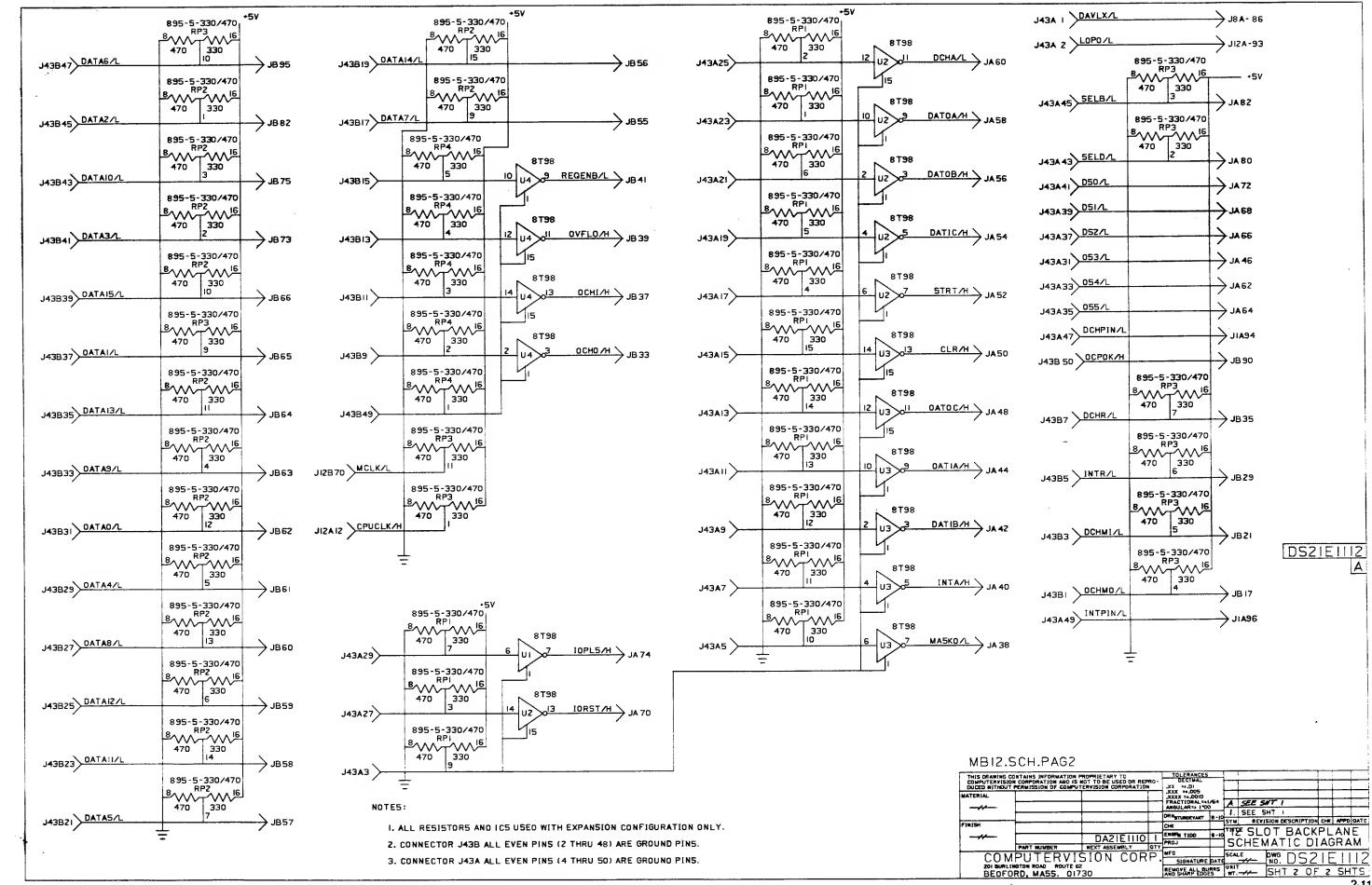
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- 3. ARTWORK MASTER WILL BE SUPPLIED TO VENDOR BY DRAFTING DEPT.
- 4. MATERIAL: .004 THICK FLEXIBLE VINYL ADHESIVE BACK.

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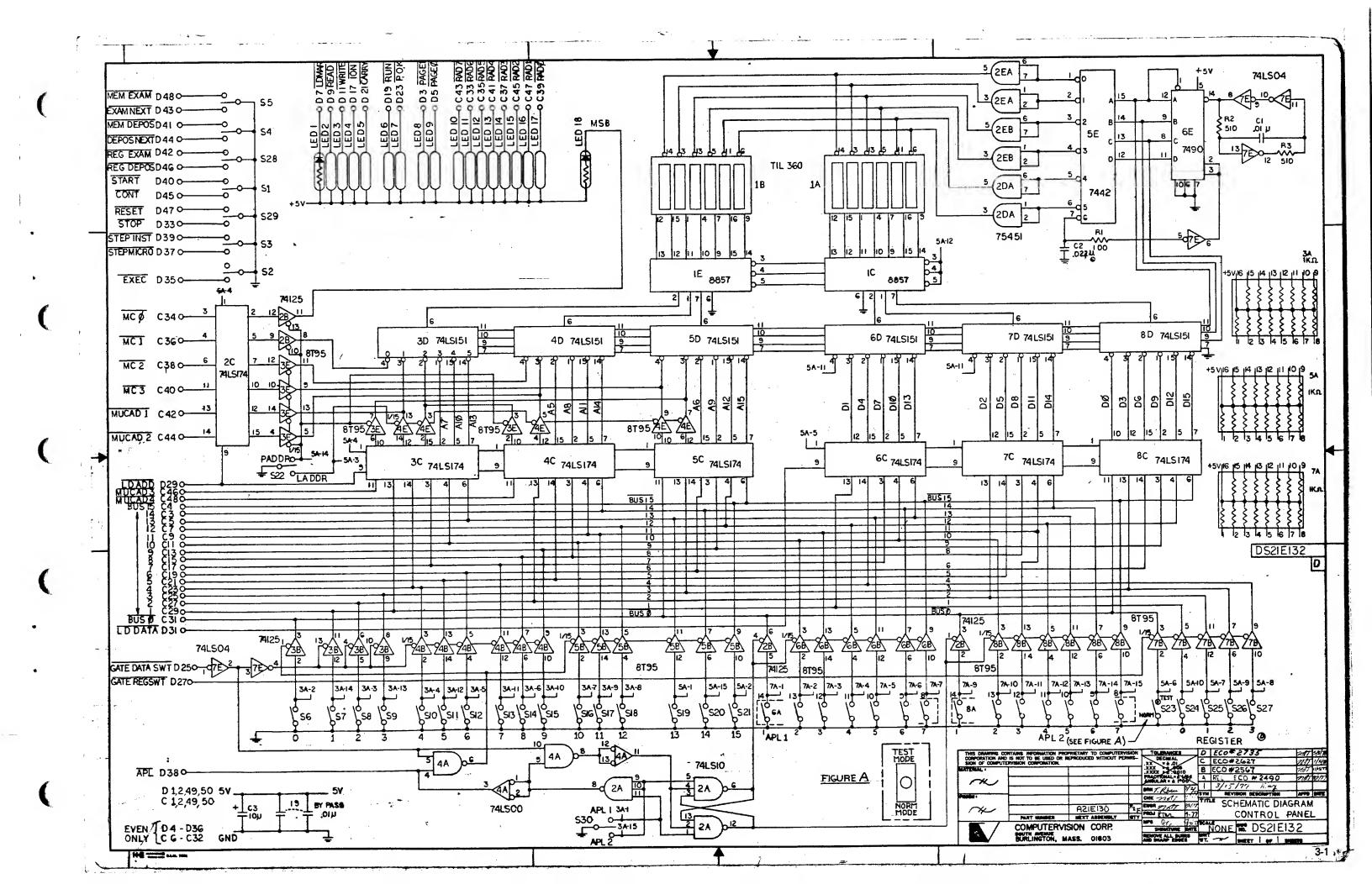




Section Three Control Panel

Maintenance Control Panel (MCP)(Rev.D) DS21E132

3-1

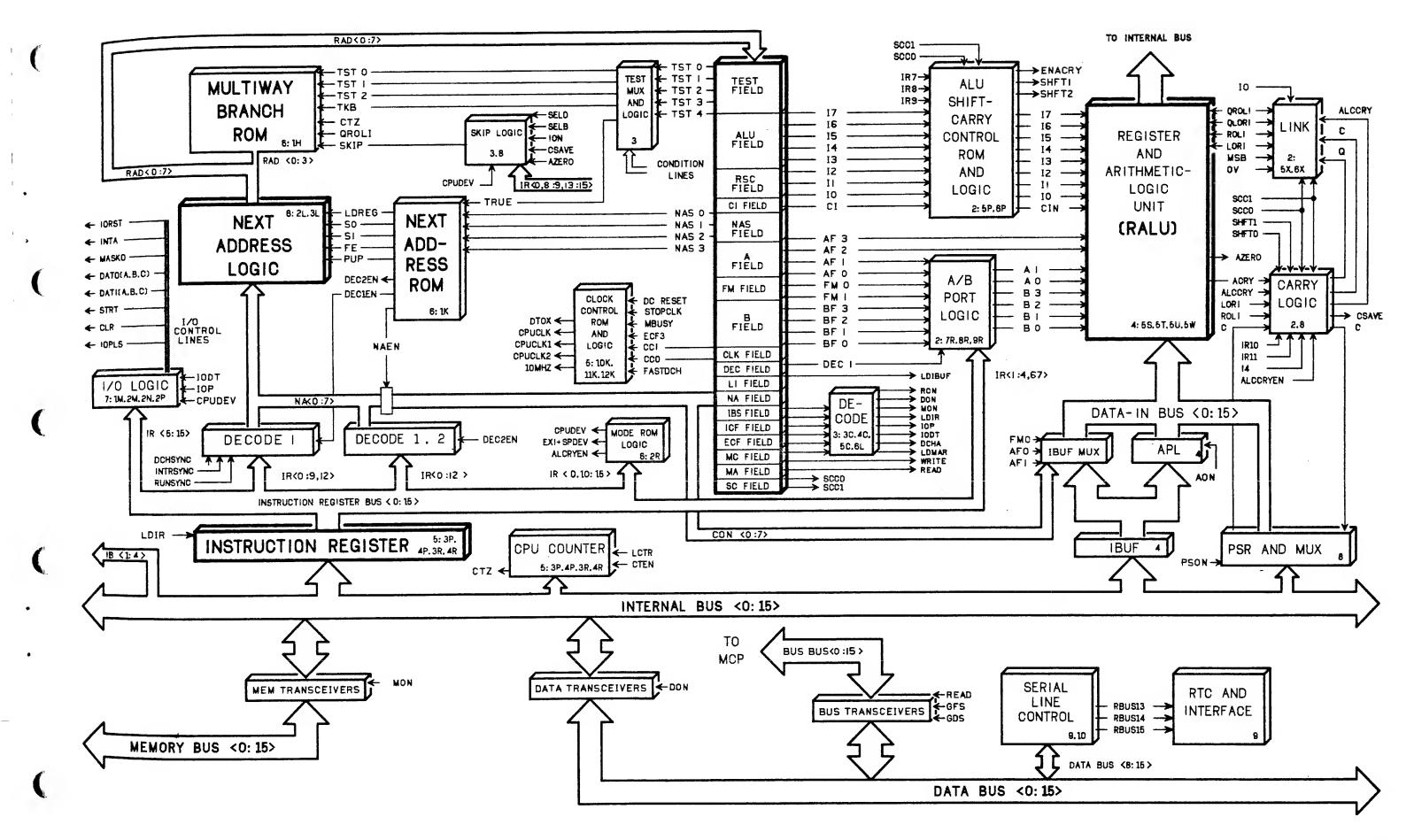


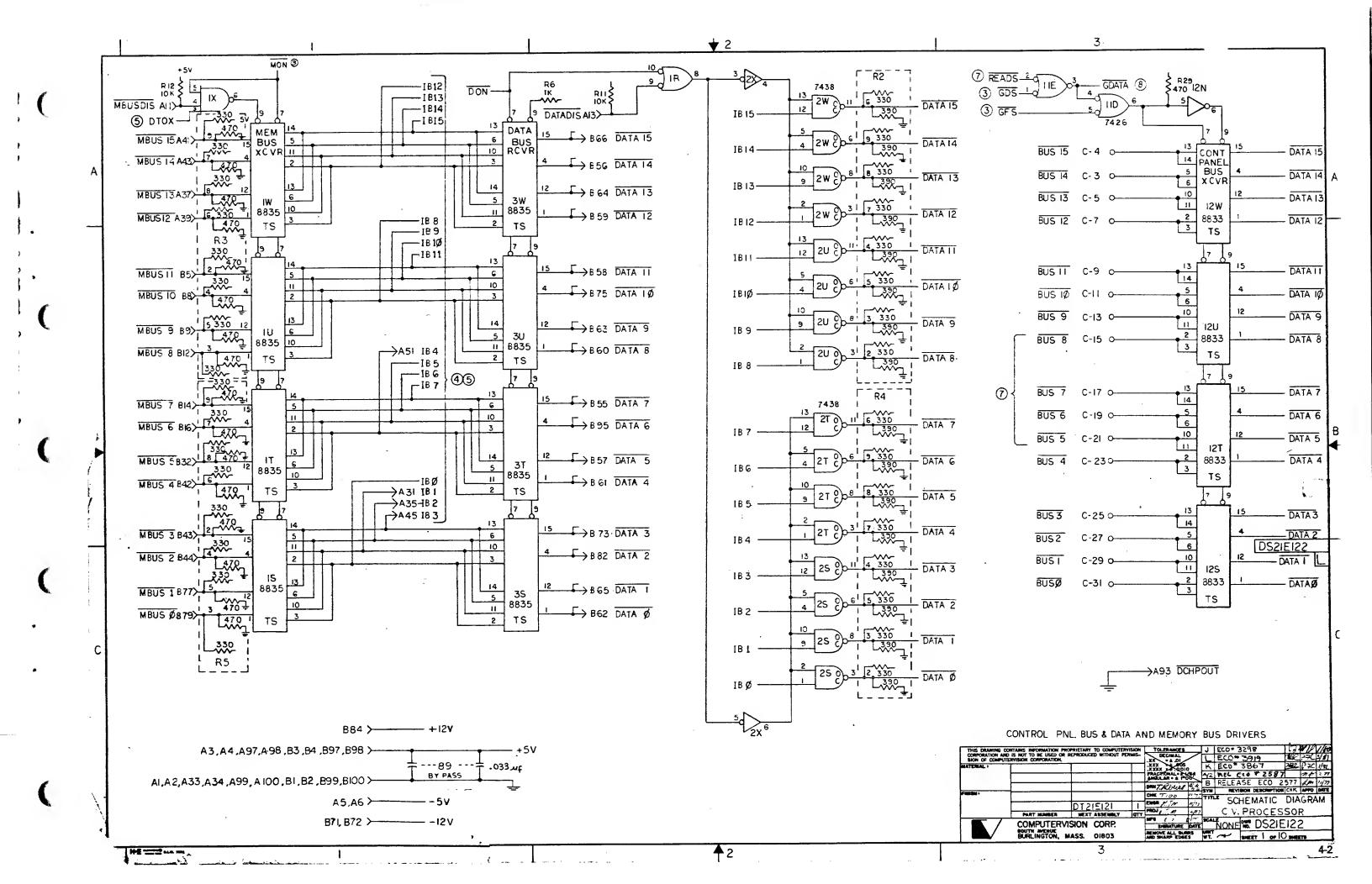
Section 4 Modules

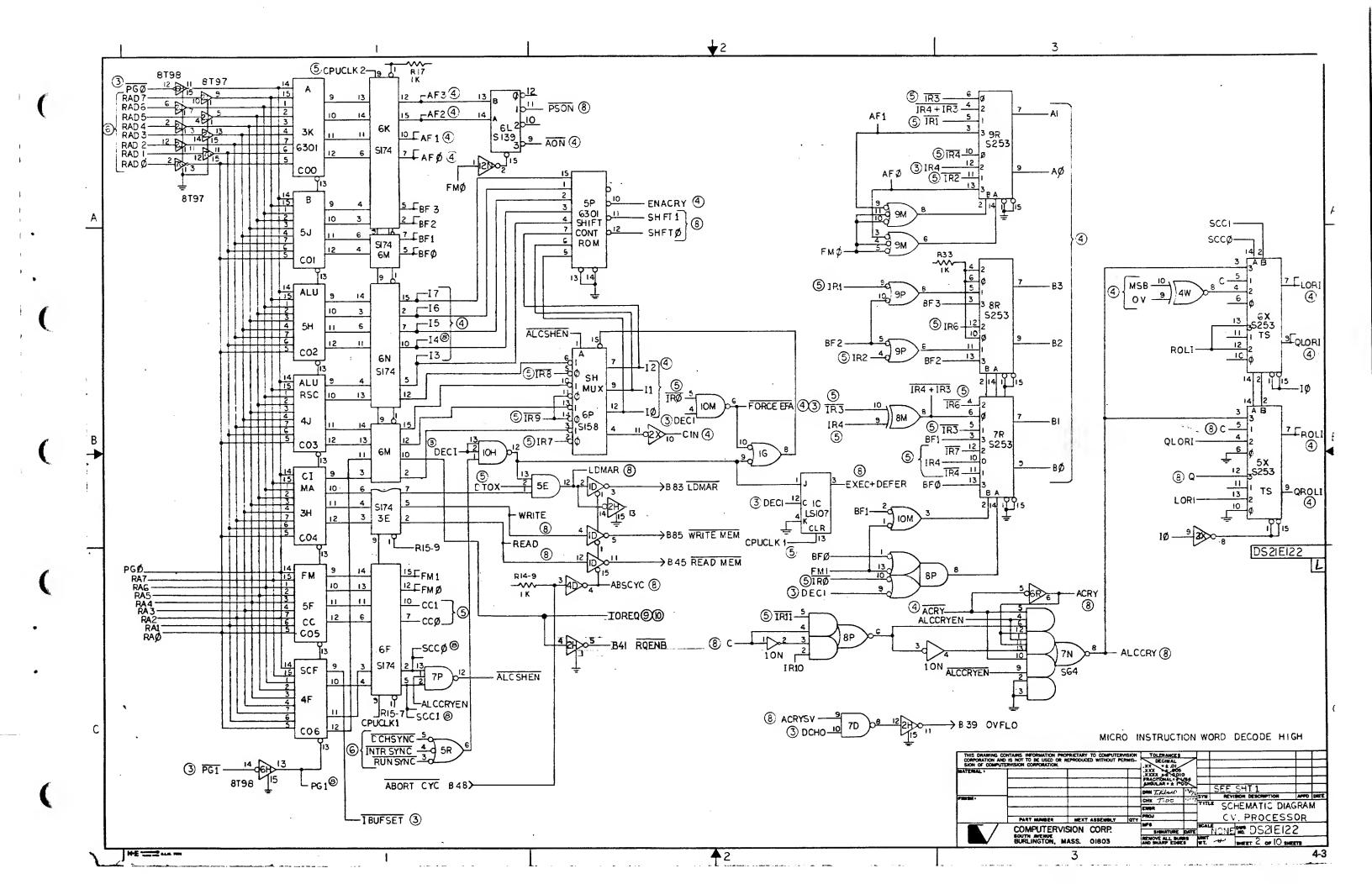
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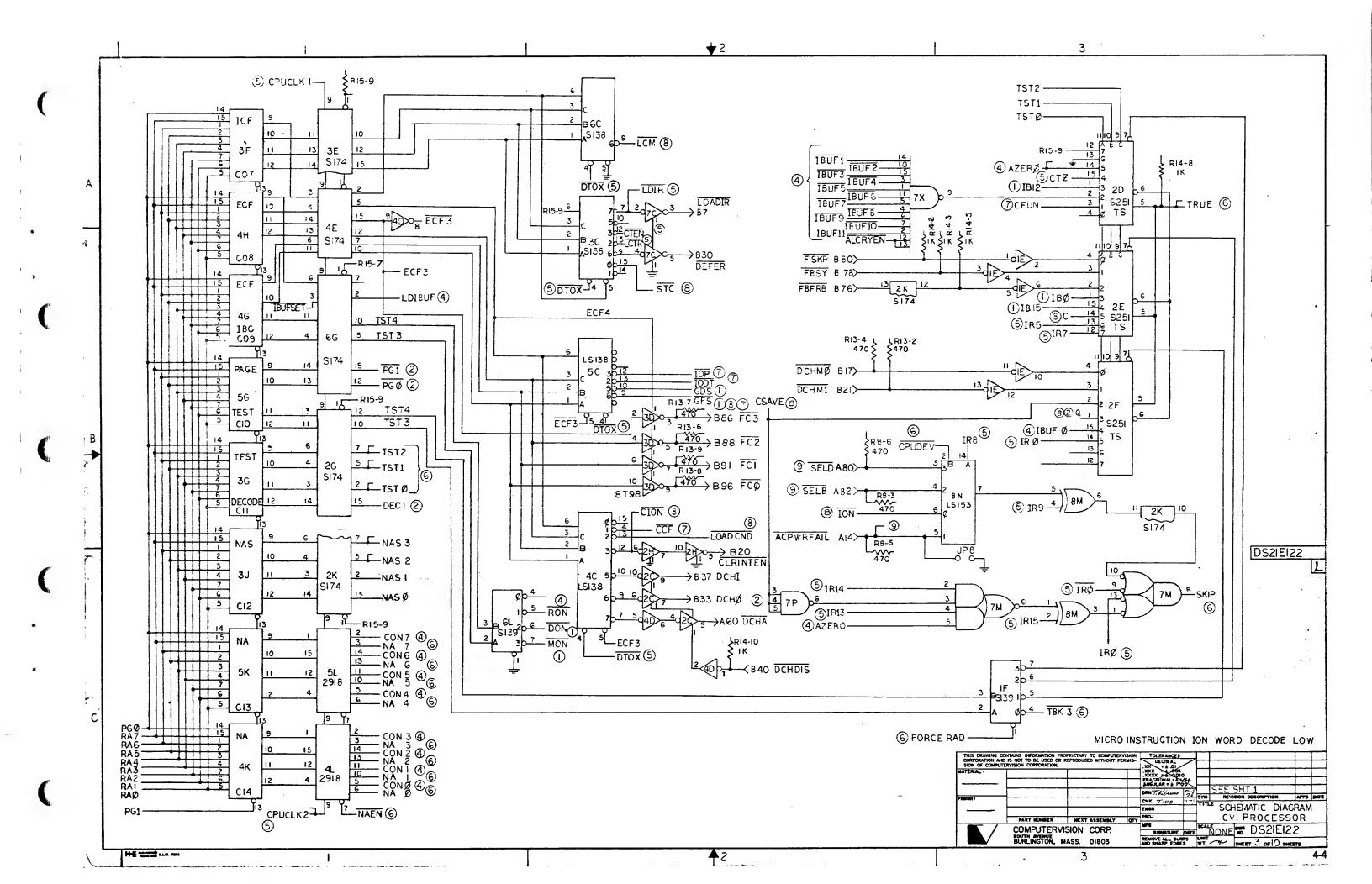
Computervision Processor, Schematic Diagram

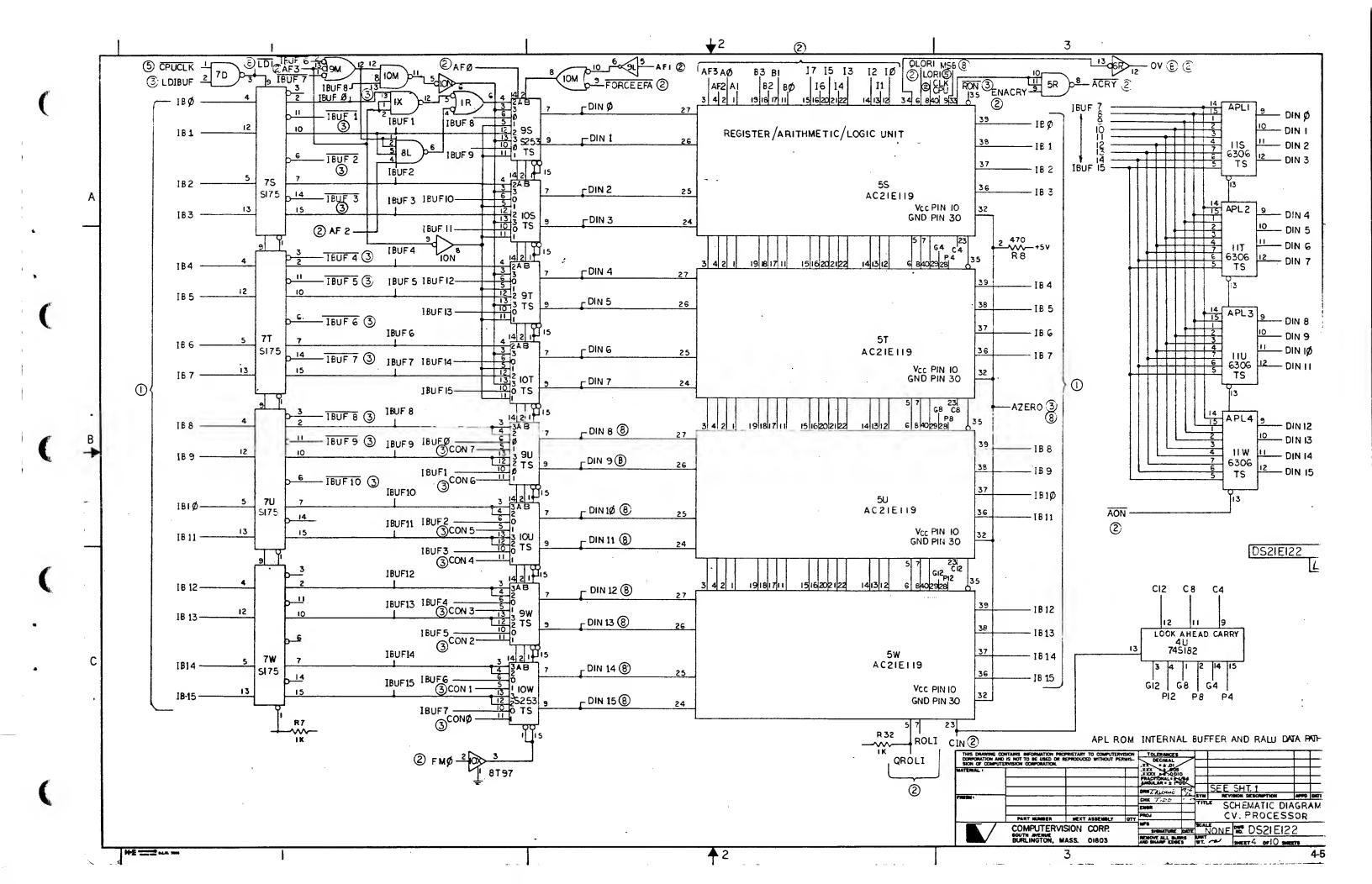
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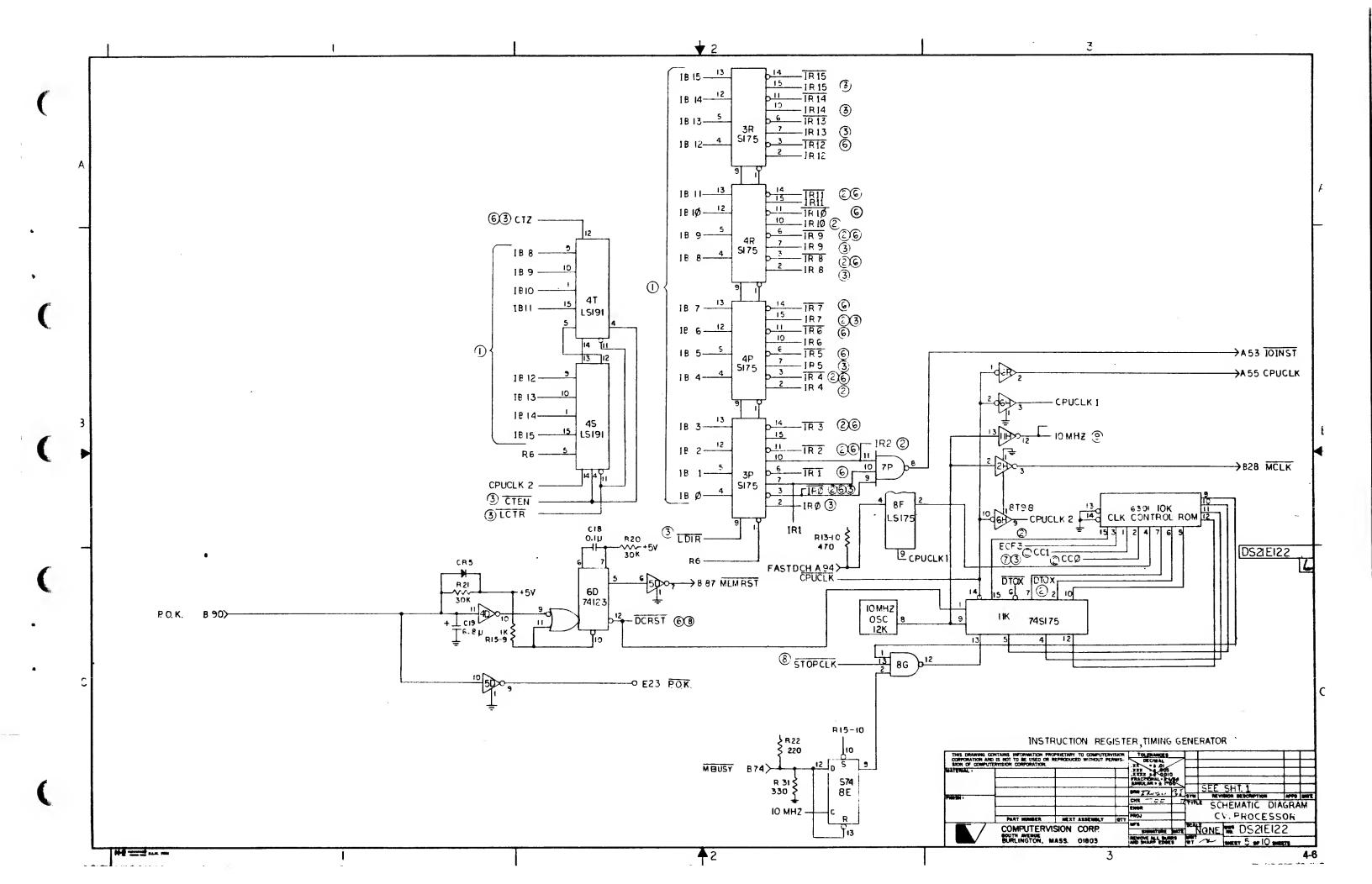


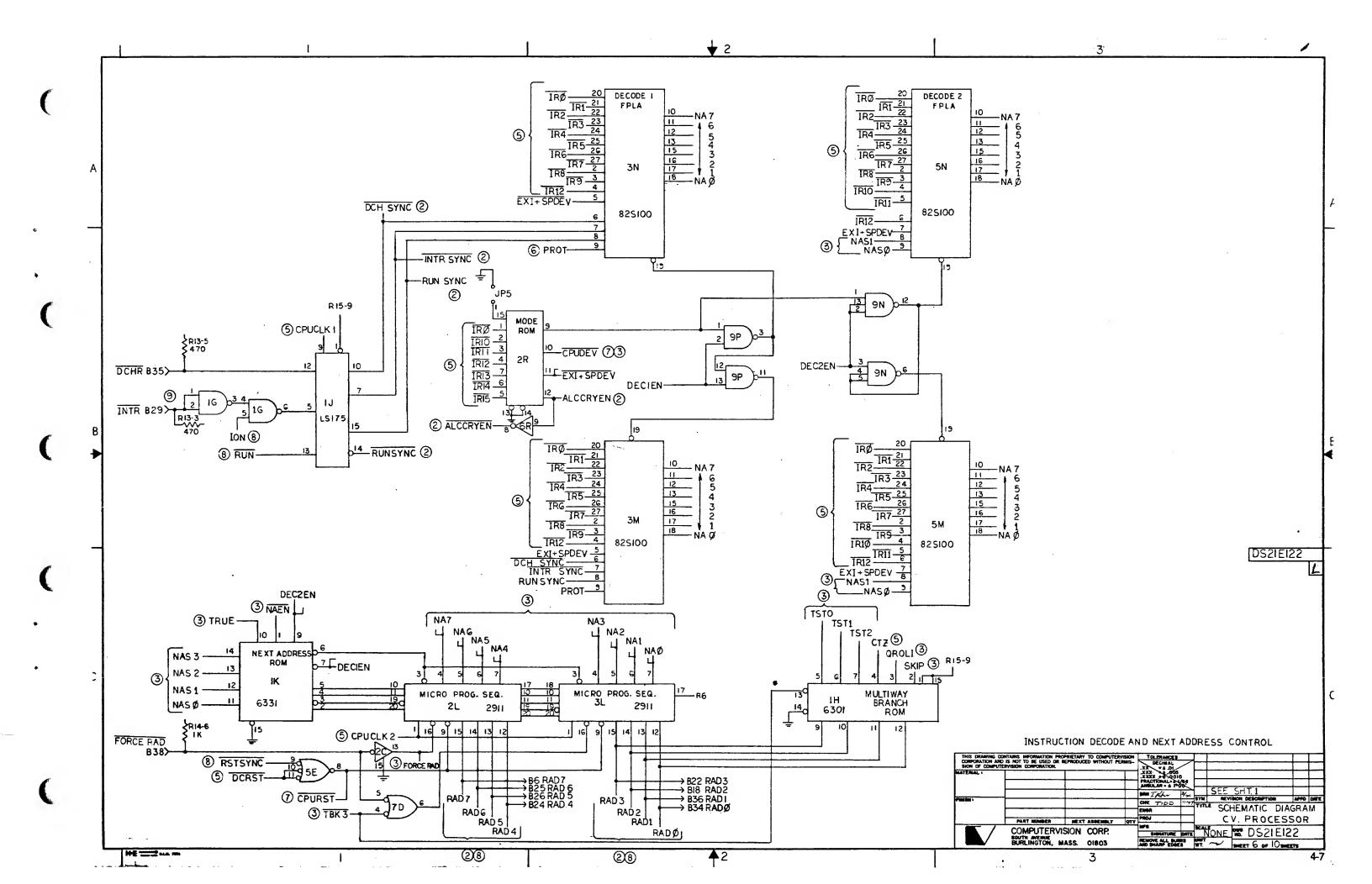


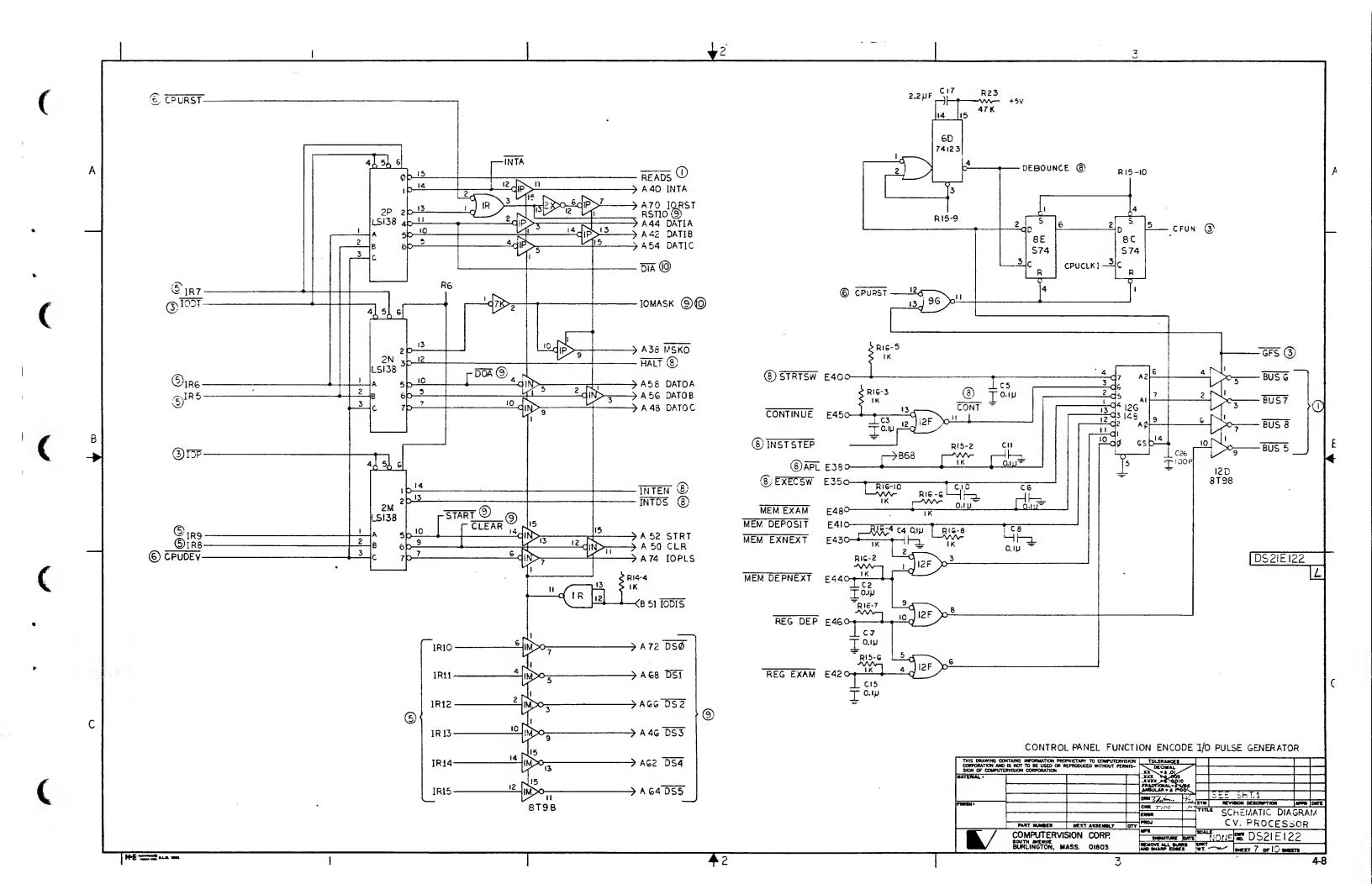


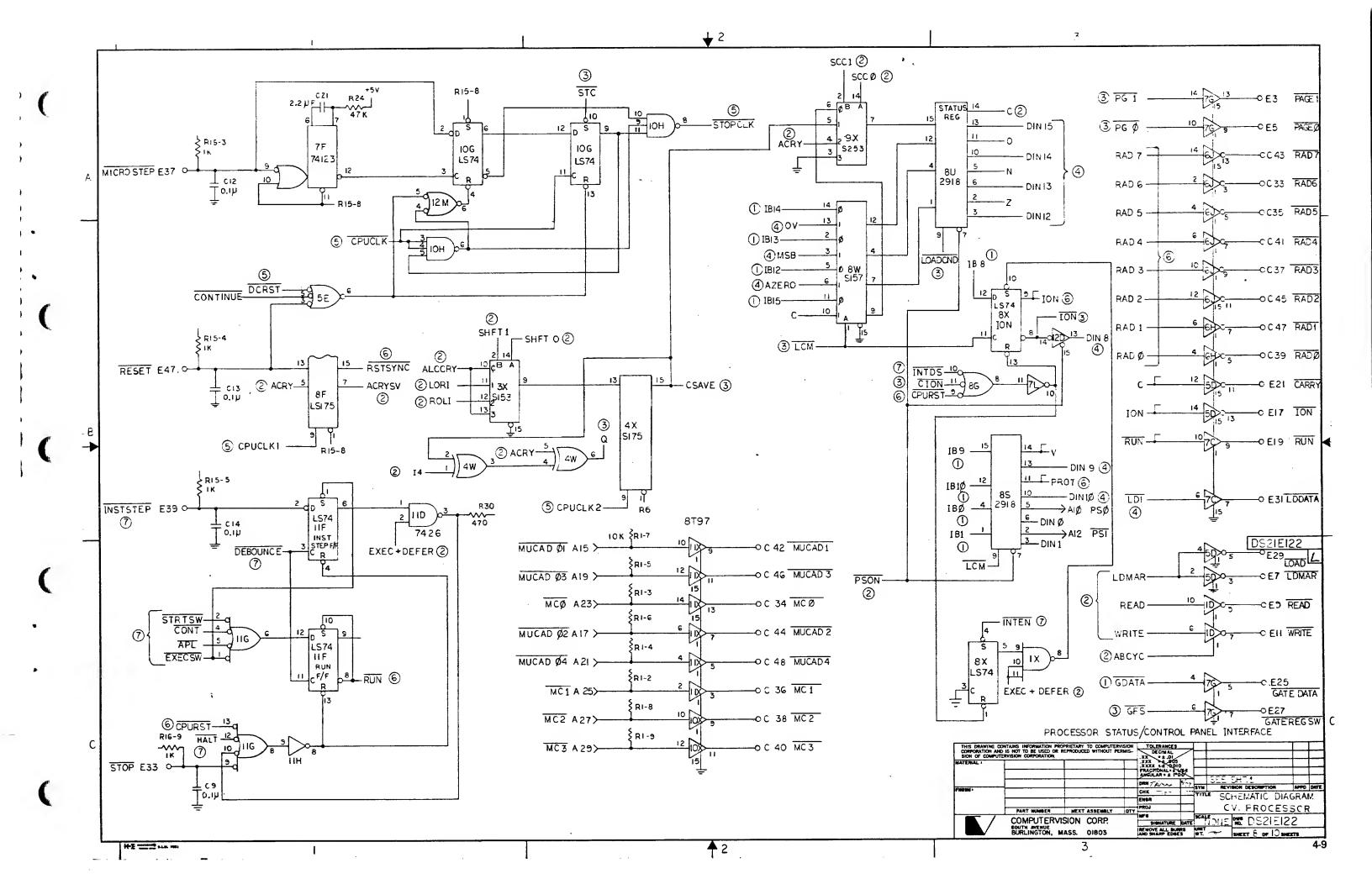


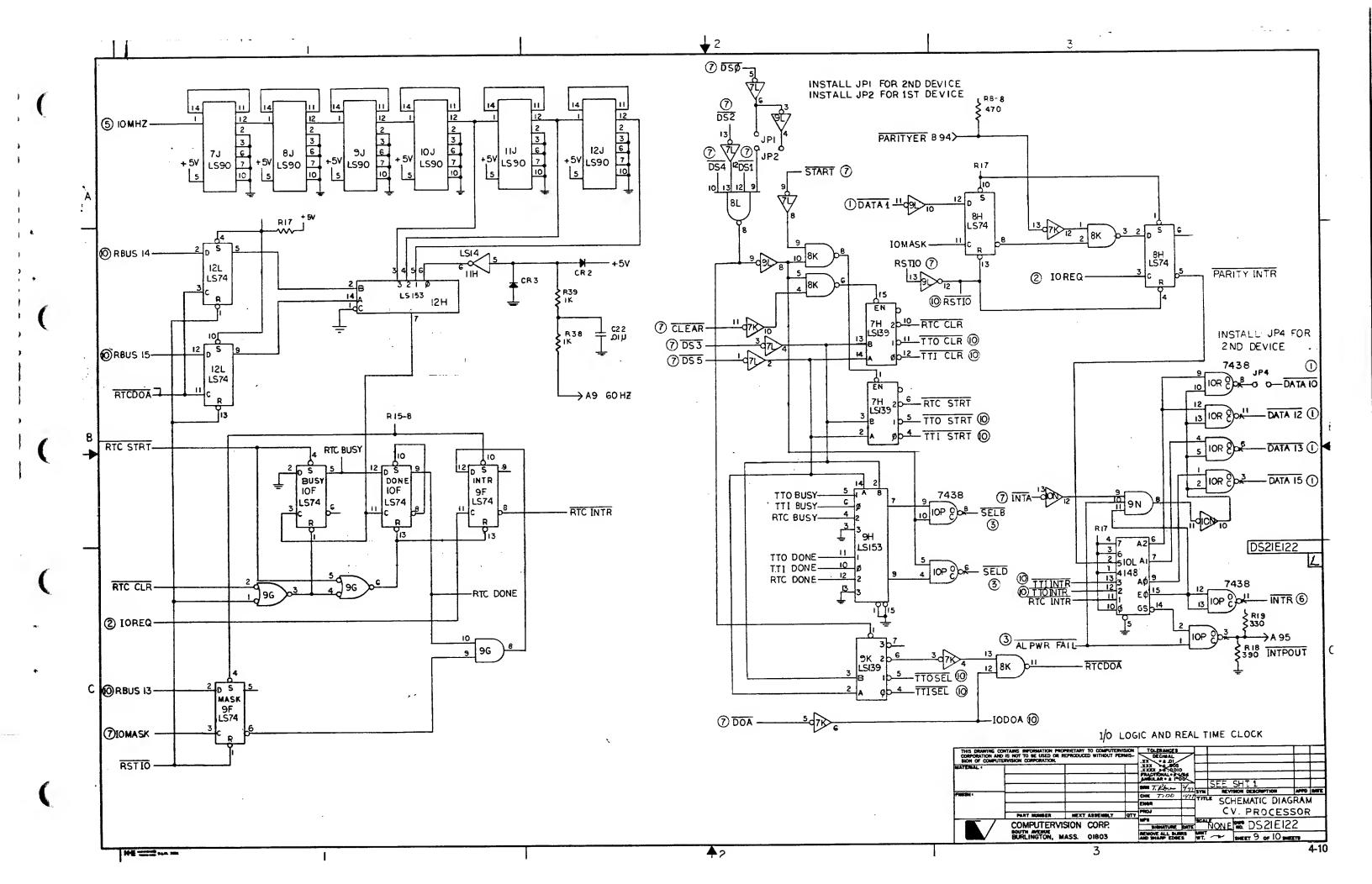


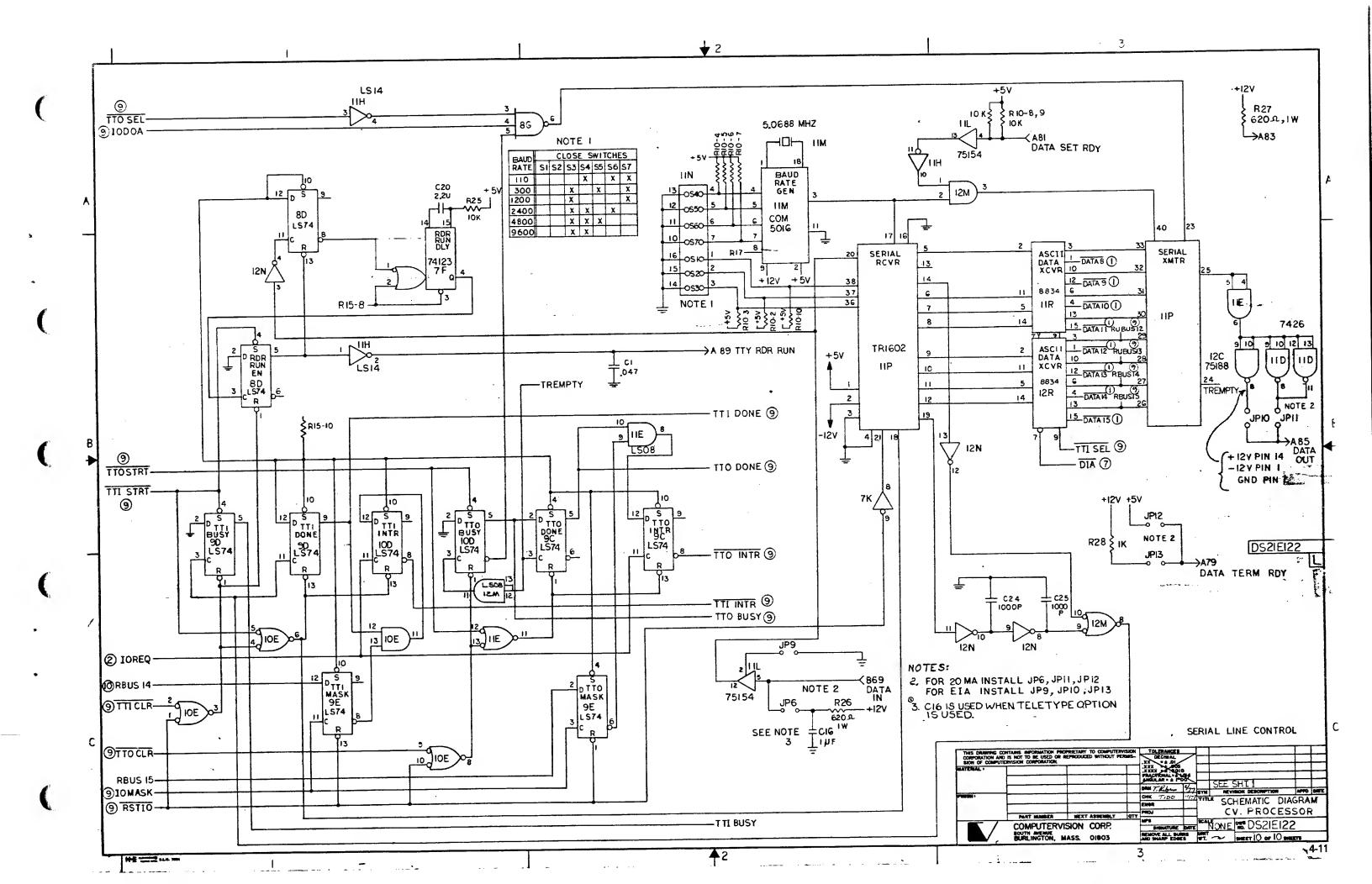












Microprogram Flow Chart

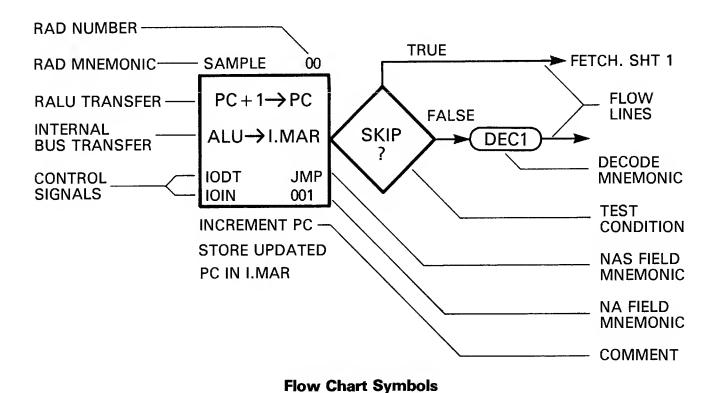
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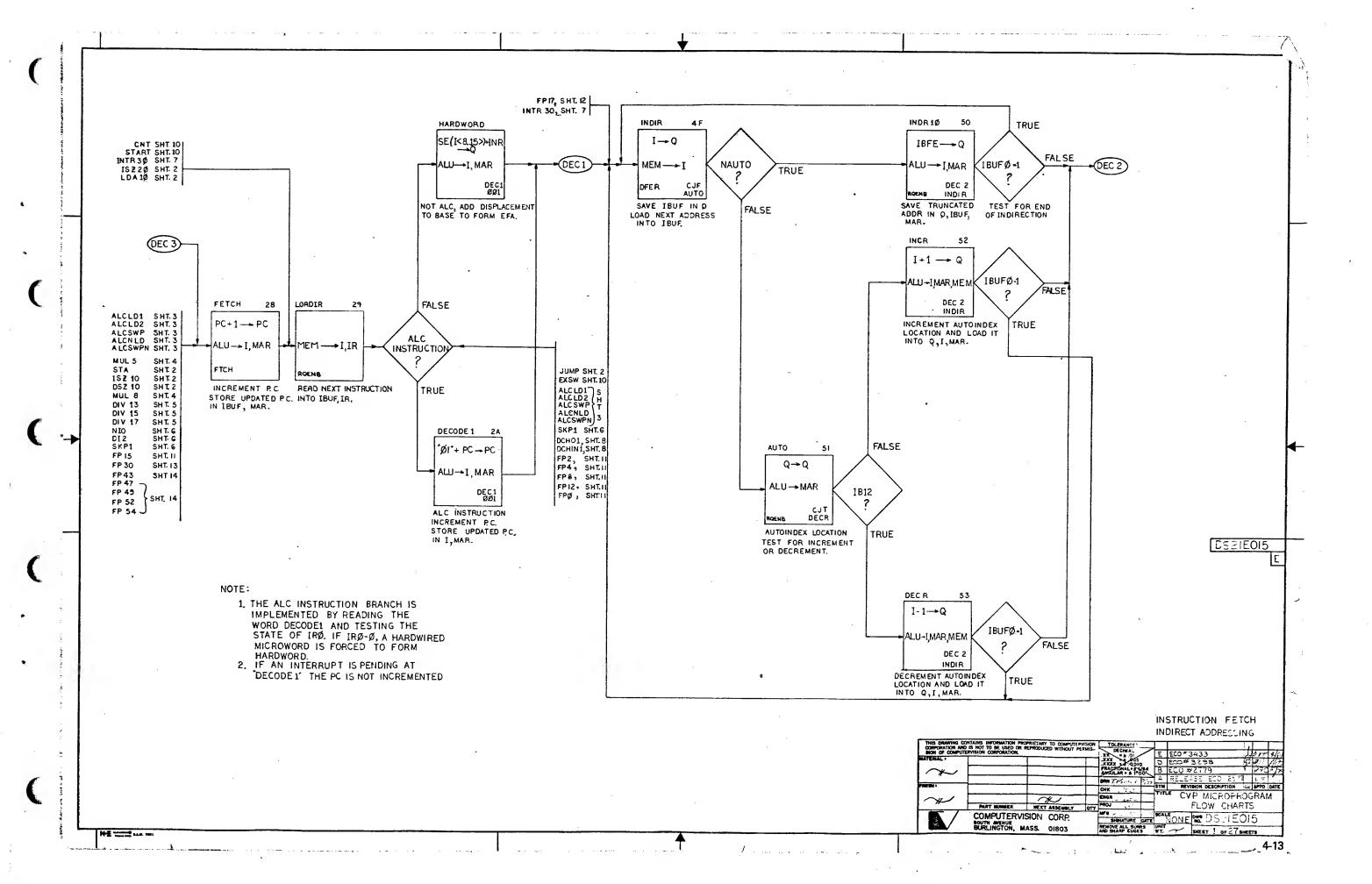
Microprogram Flow Chart

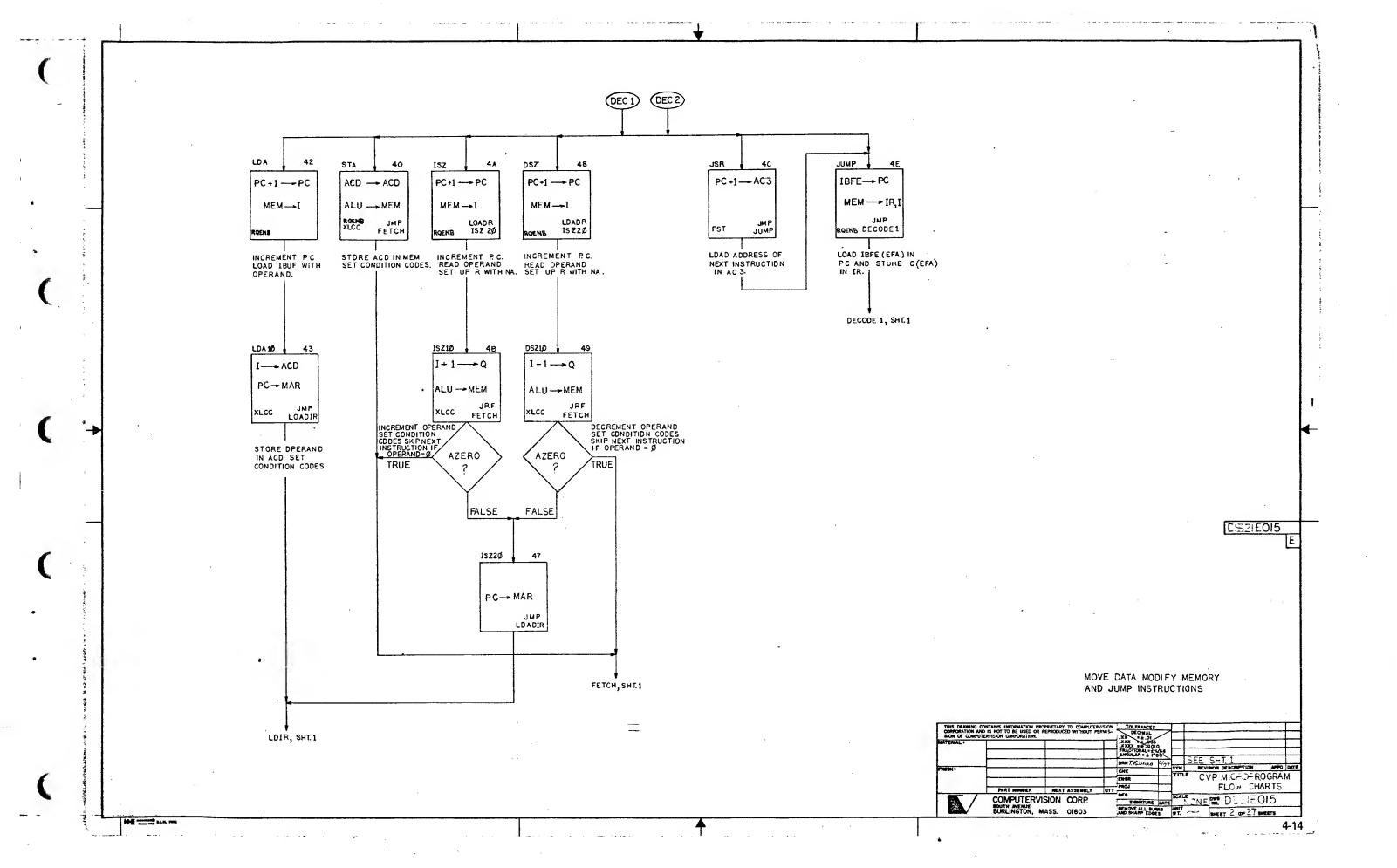
Interpreting the Flow Charts

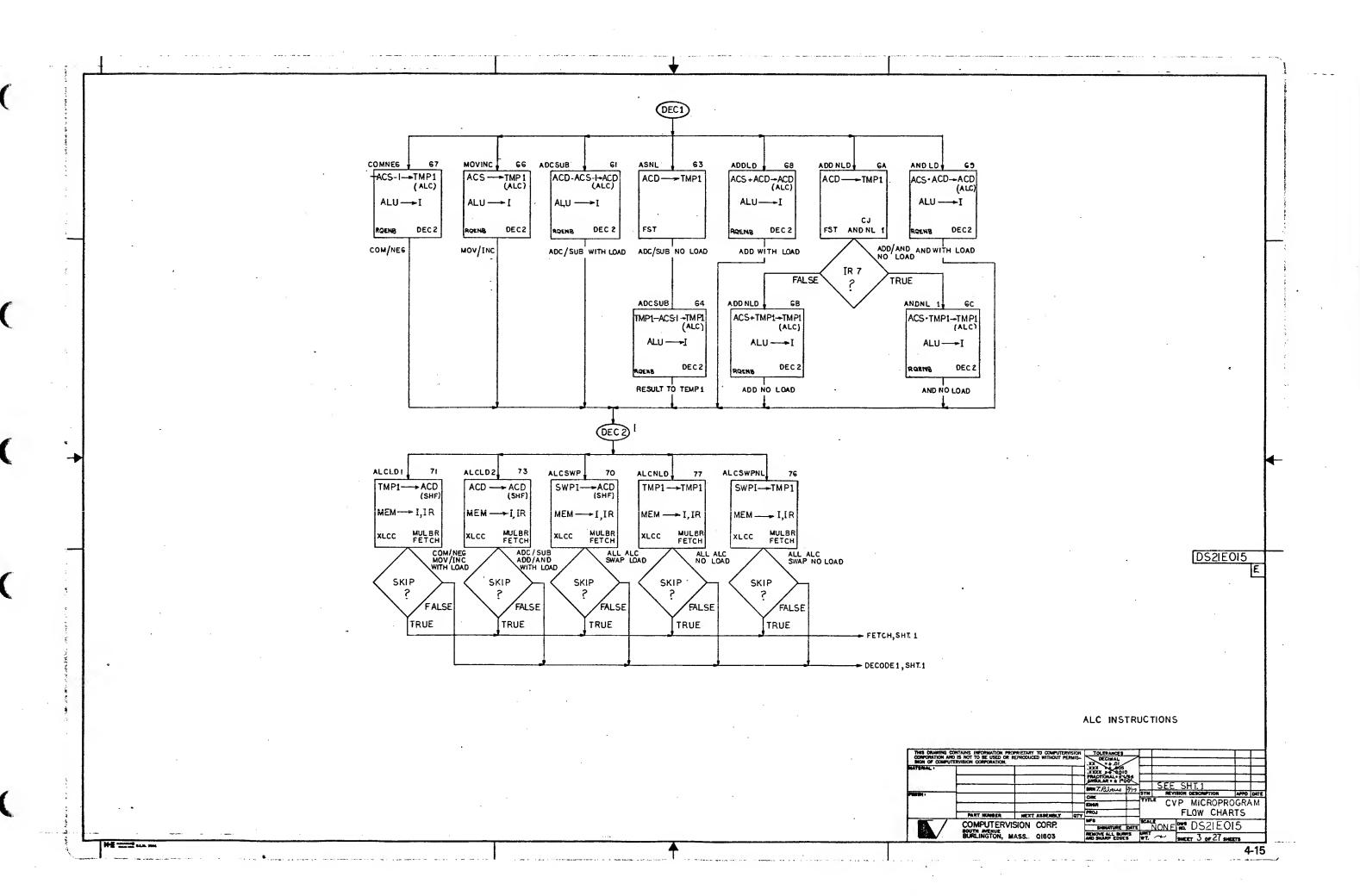
The flow charts are divided into three sections. The first 10 pages (Sheets 1-10) show the operation code for the CPU. The next four pages (Sheets 11-14) show the operation code for the FPU. And the last 13 pages (Sheets 15-27) show the code for the microdiagnostics.

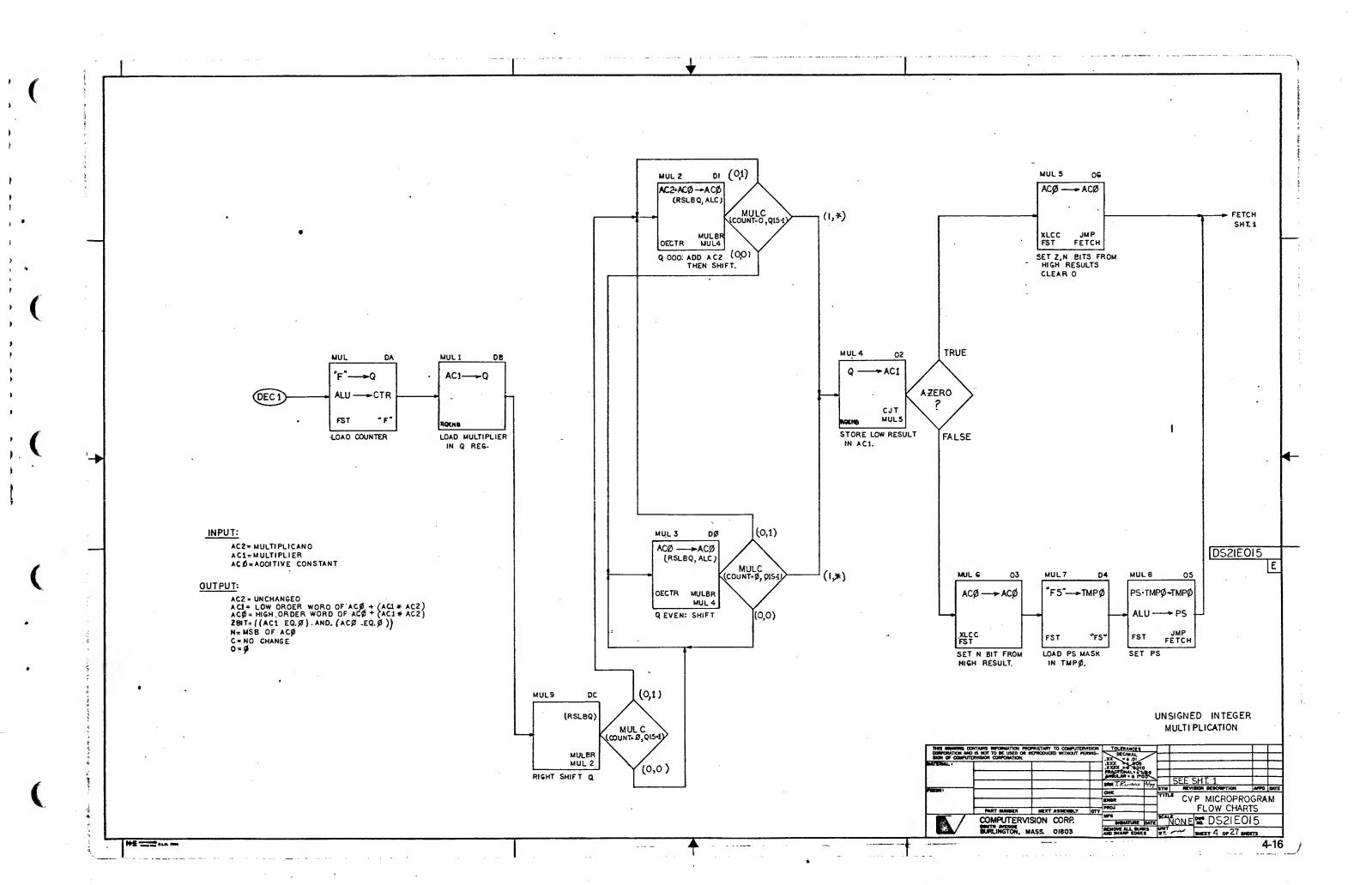
Symbols. The flow charts use three symbols: squares, diamonds, and ovals. The square represents the RAD currently being executed. The diamond represents a test condition. The oval indicates a decoding of the instruction. Flow lines connect these three symbols to indicate their sequential relationship. Mnemonics and comments accompanying each square also help to indicate the flow.

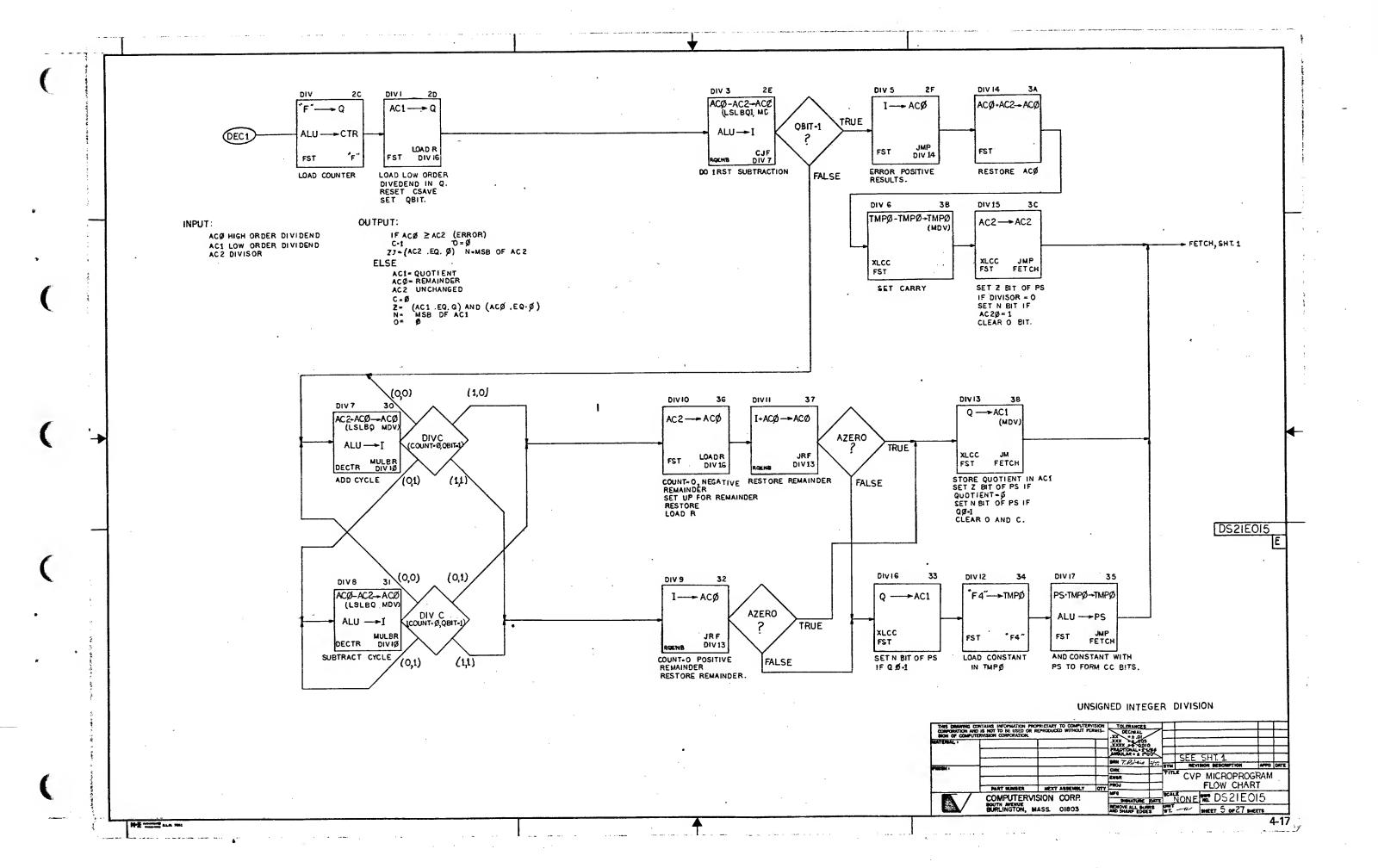


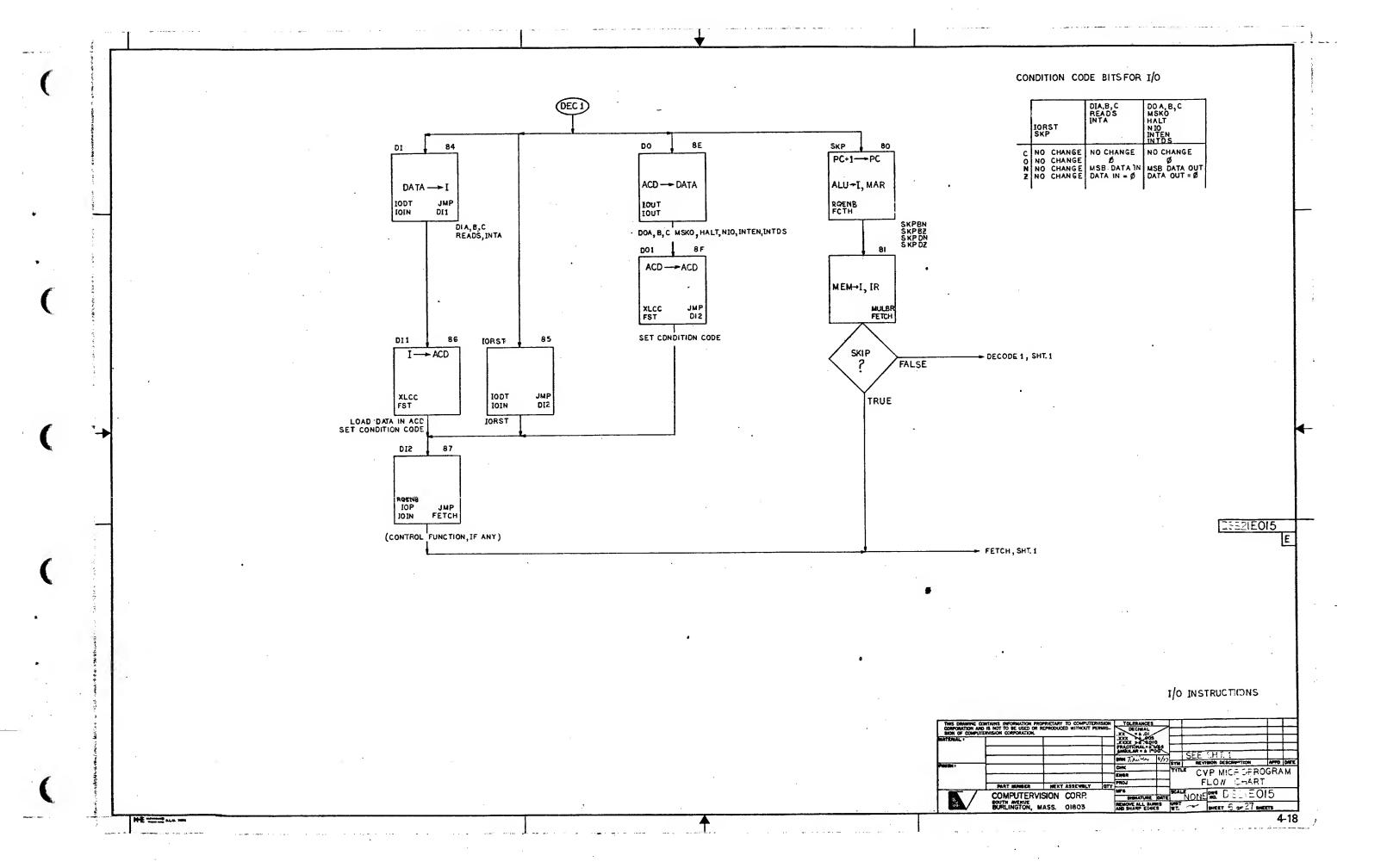


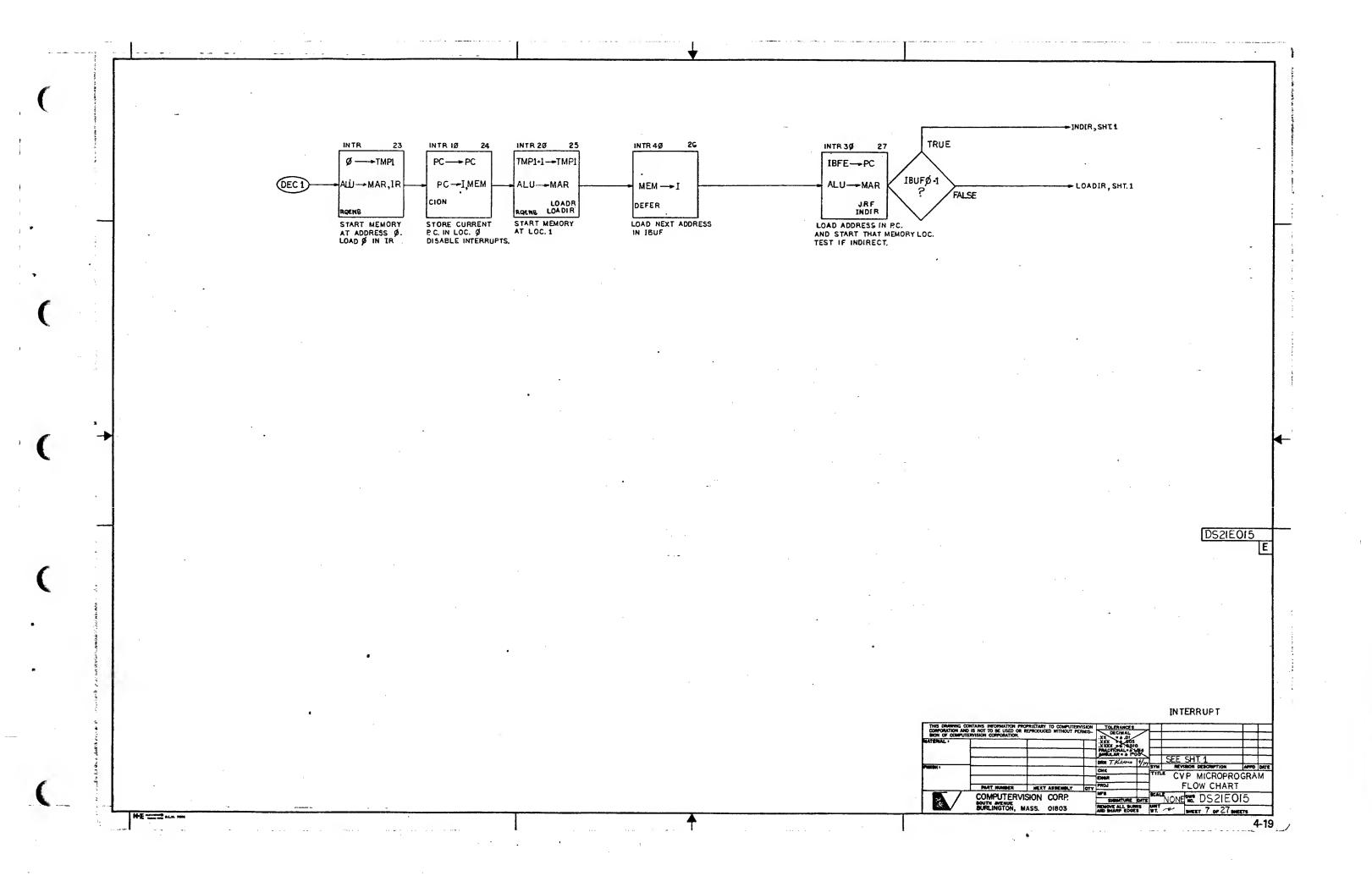


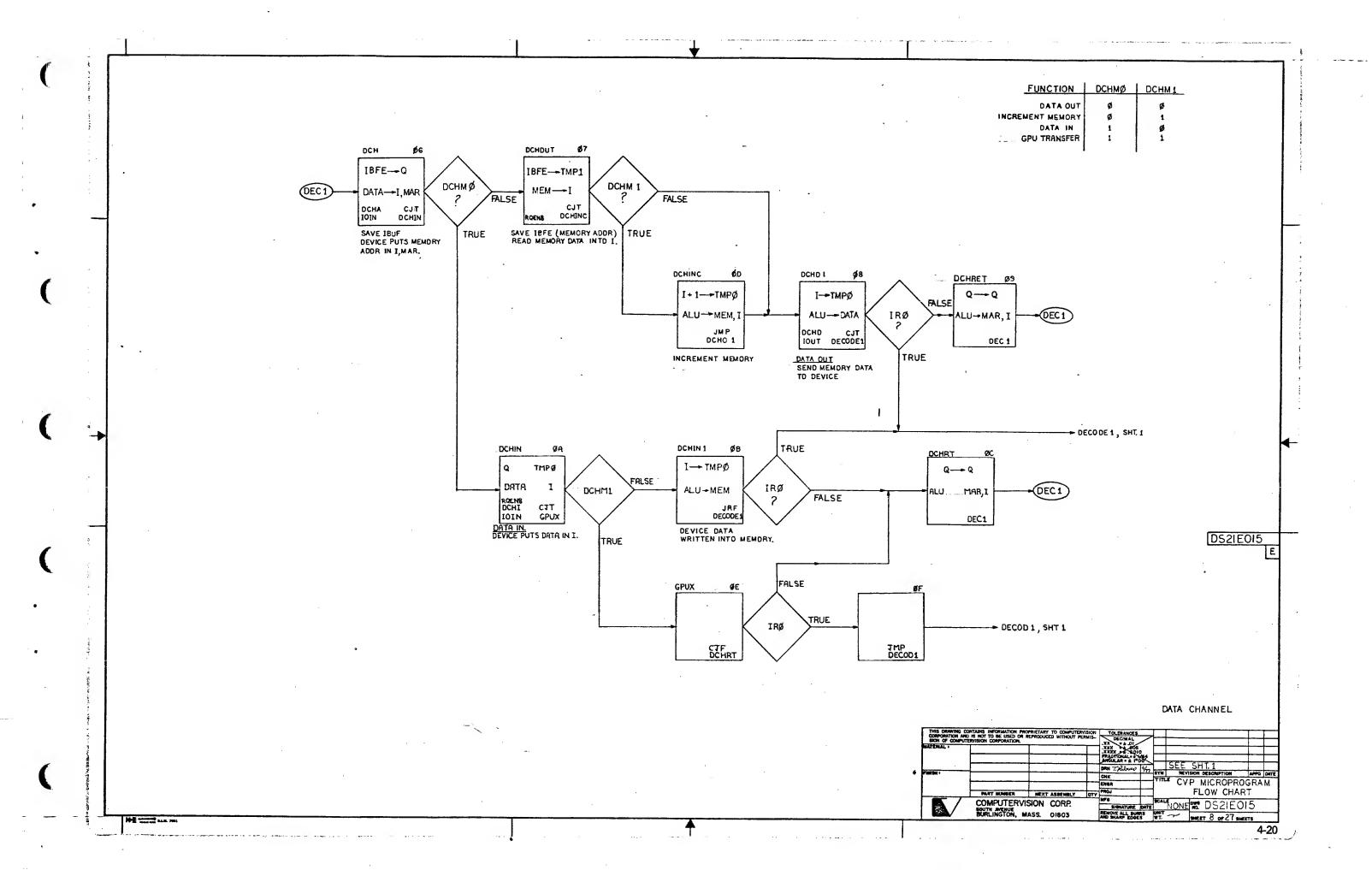


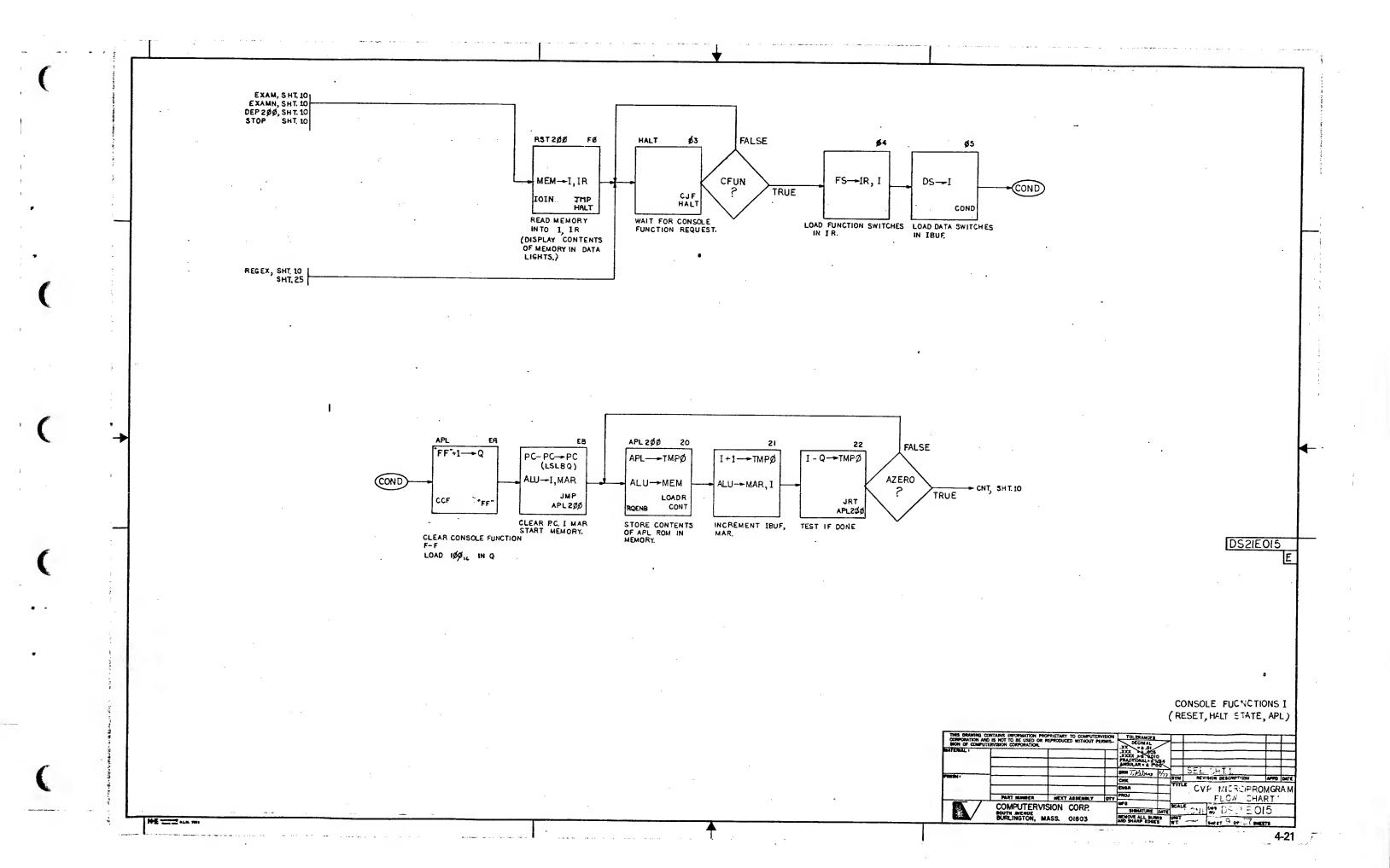


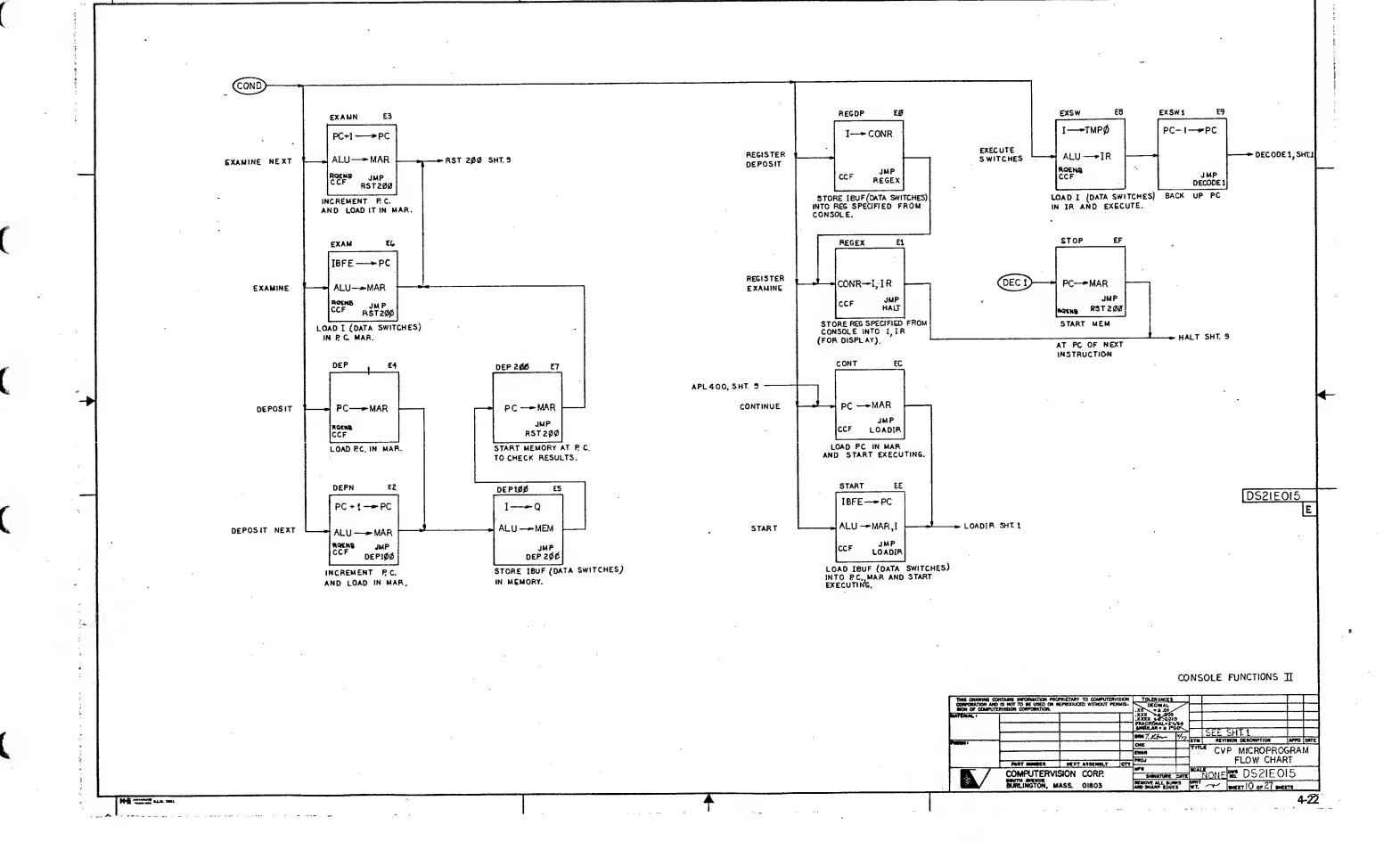


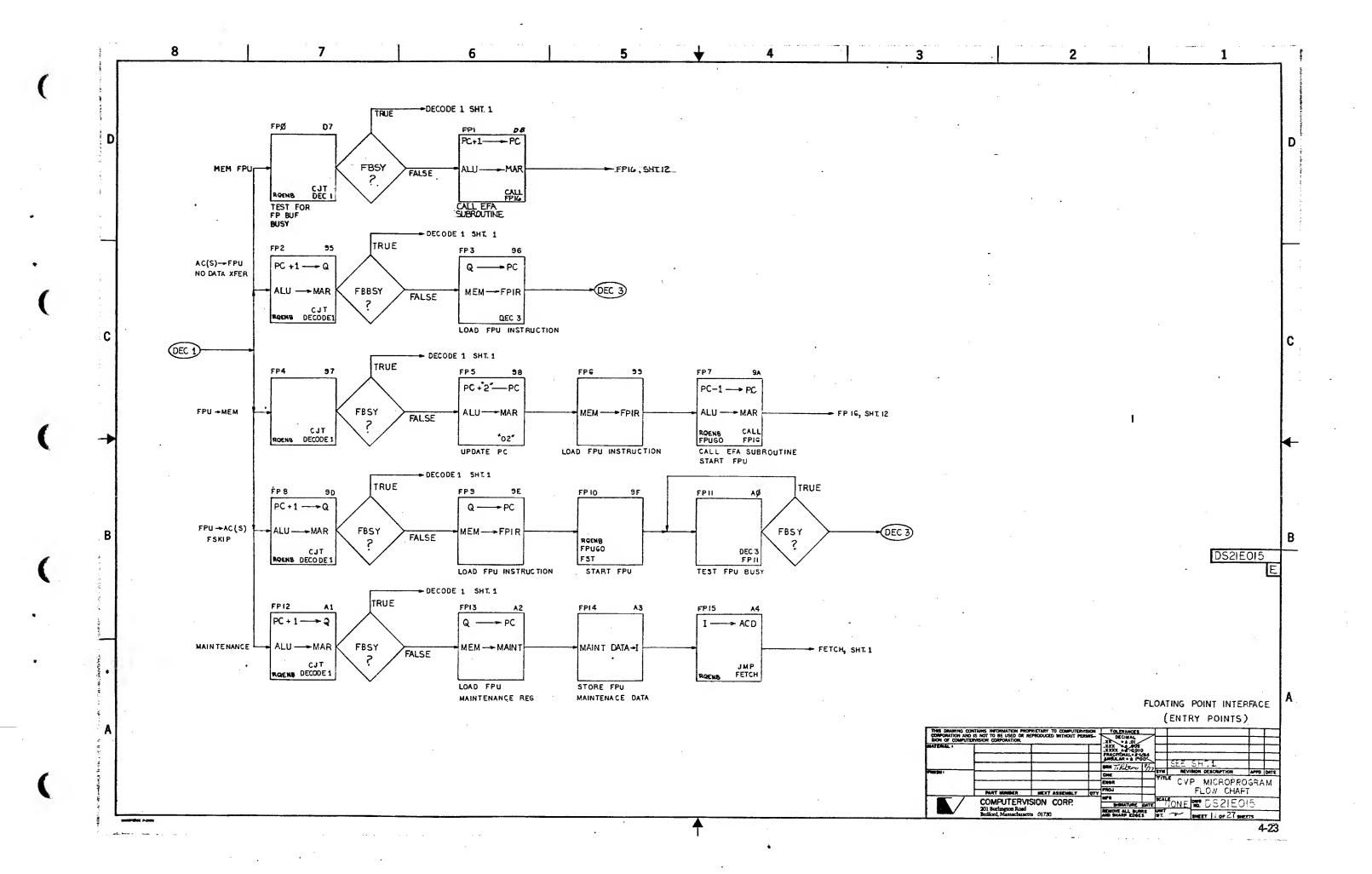


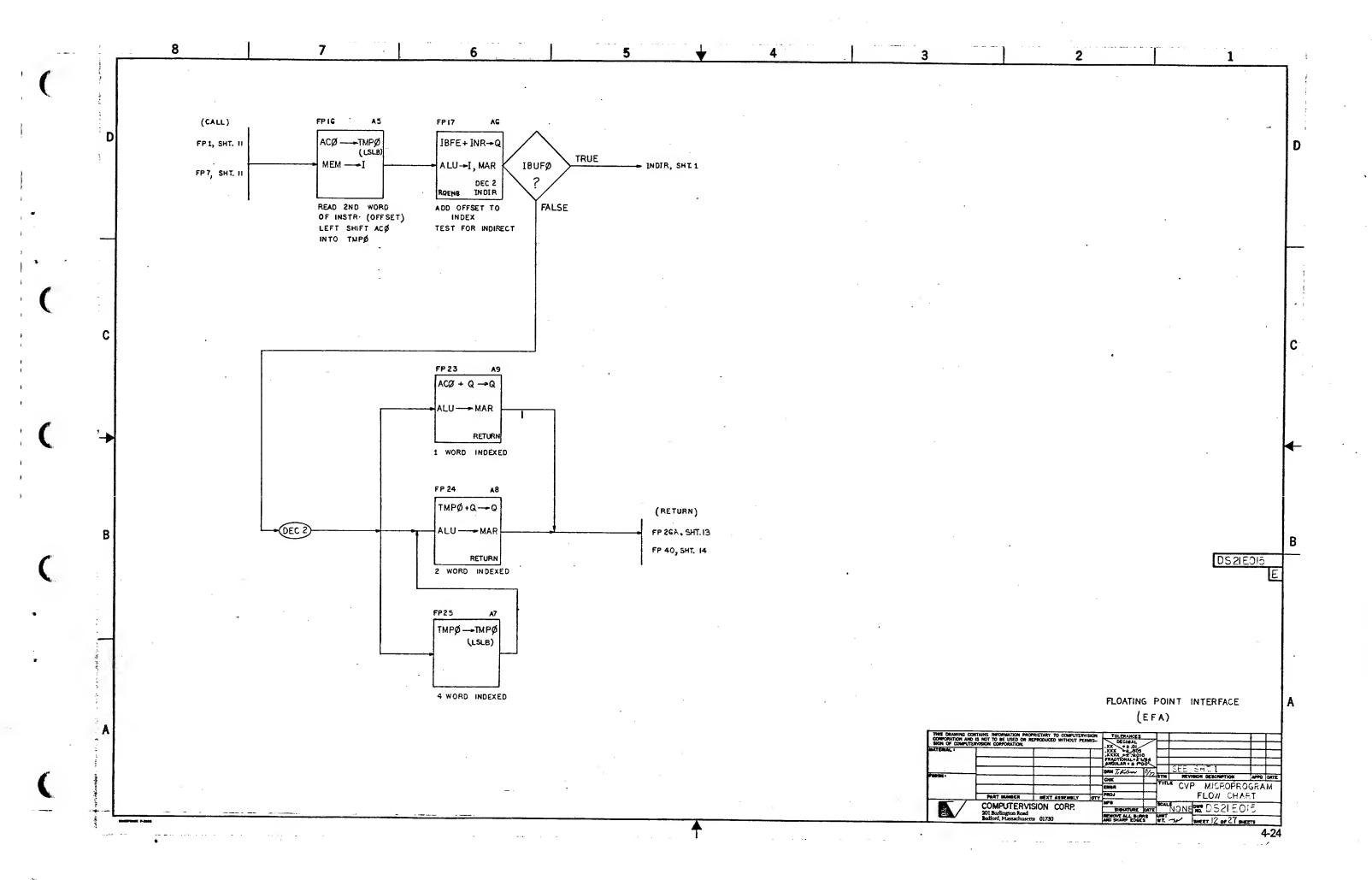


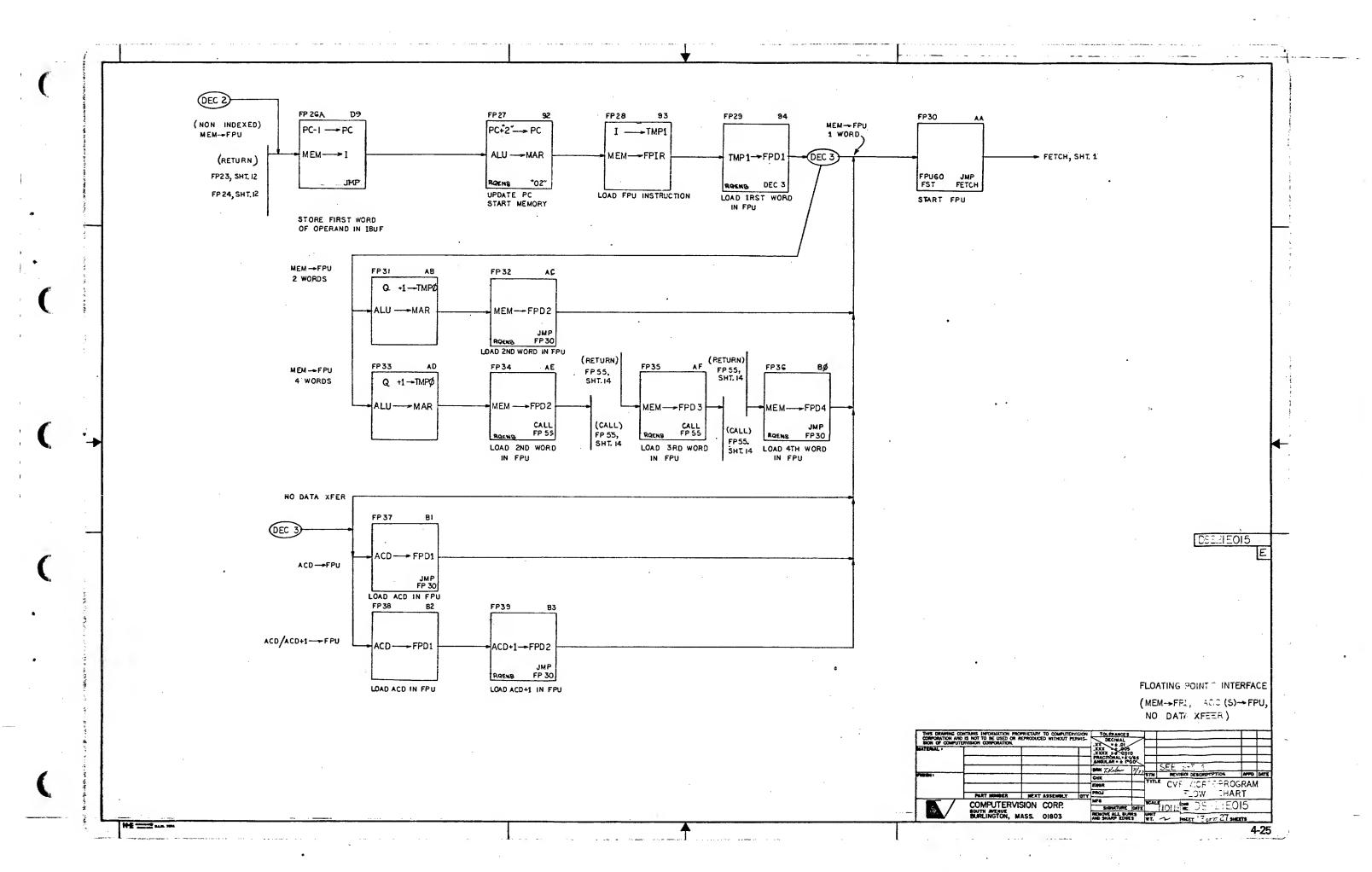


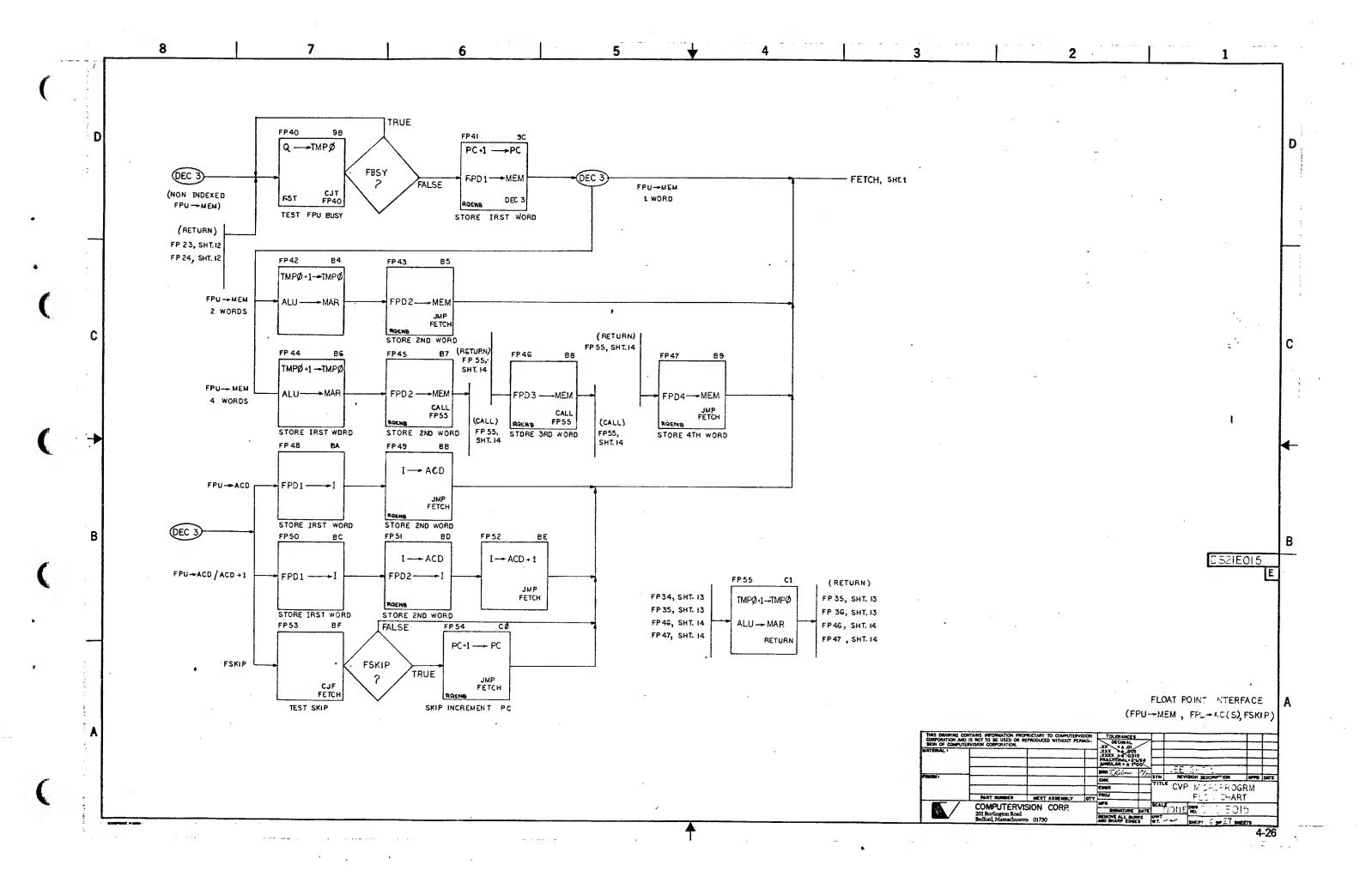


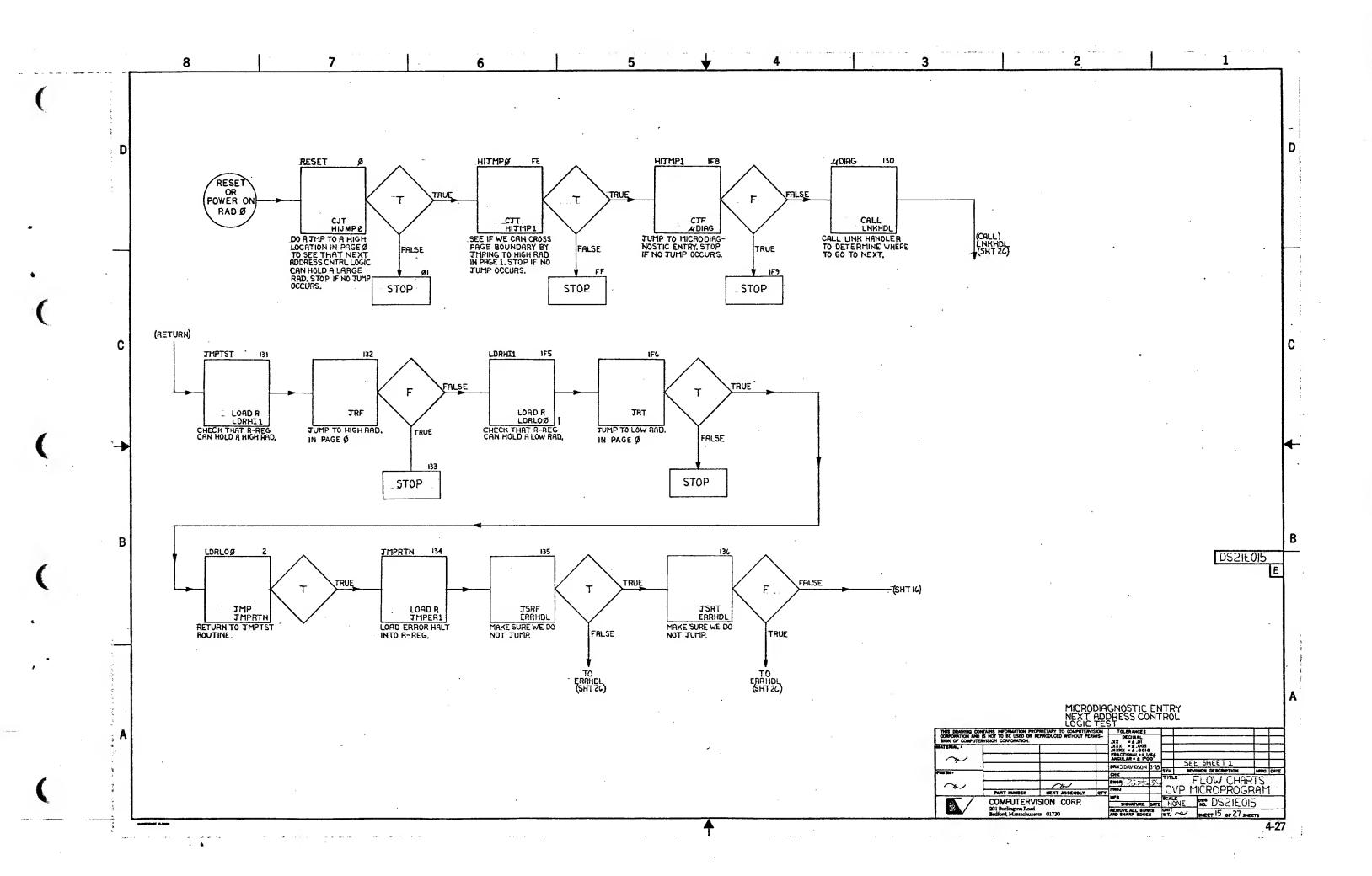


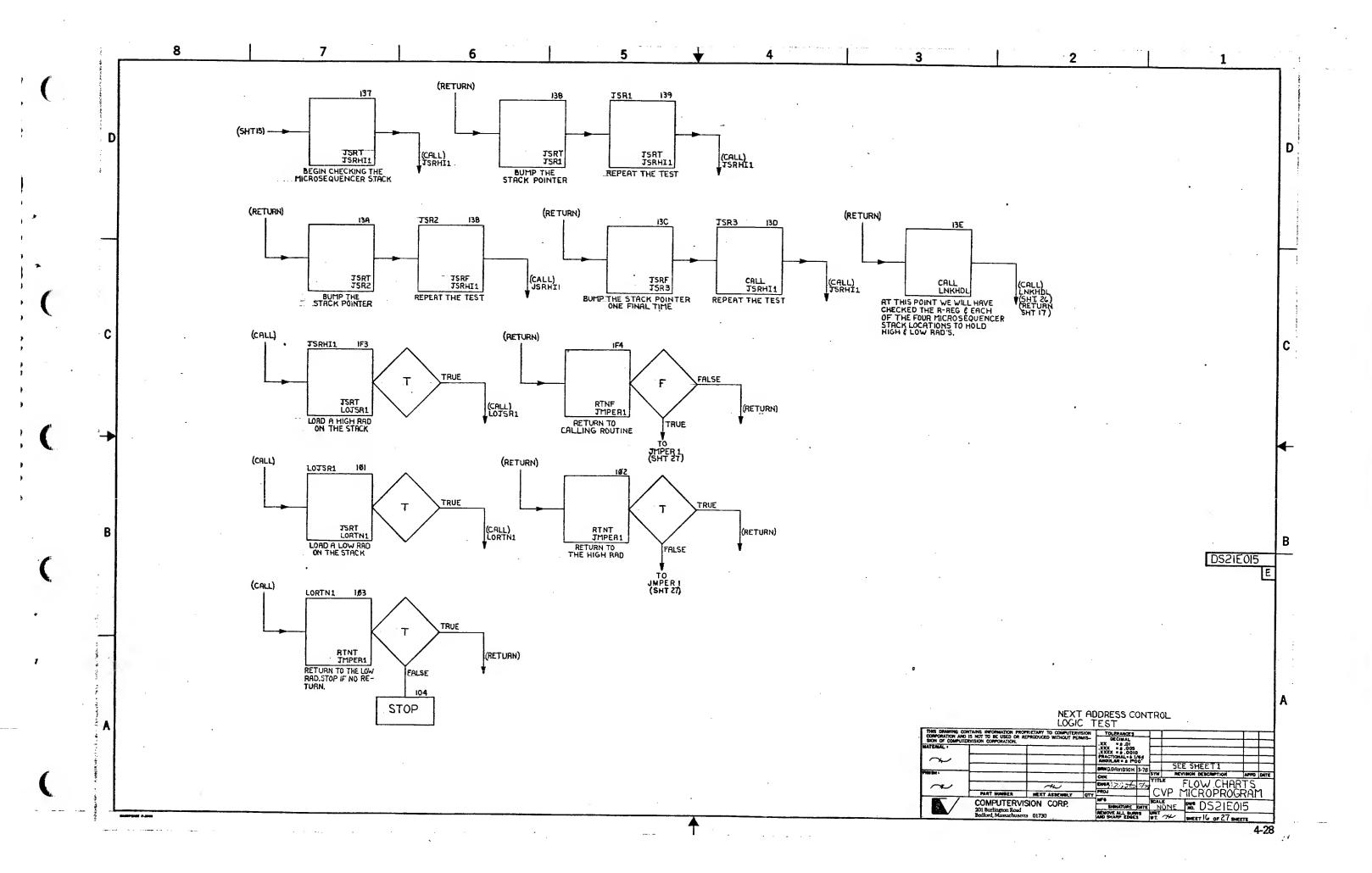


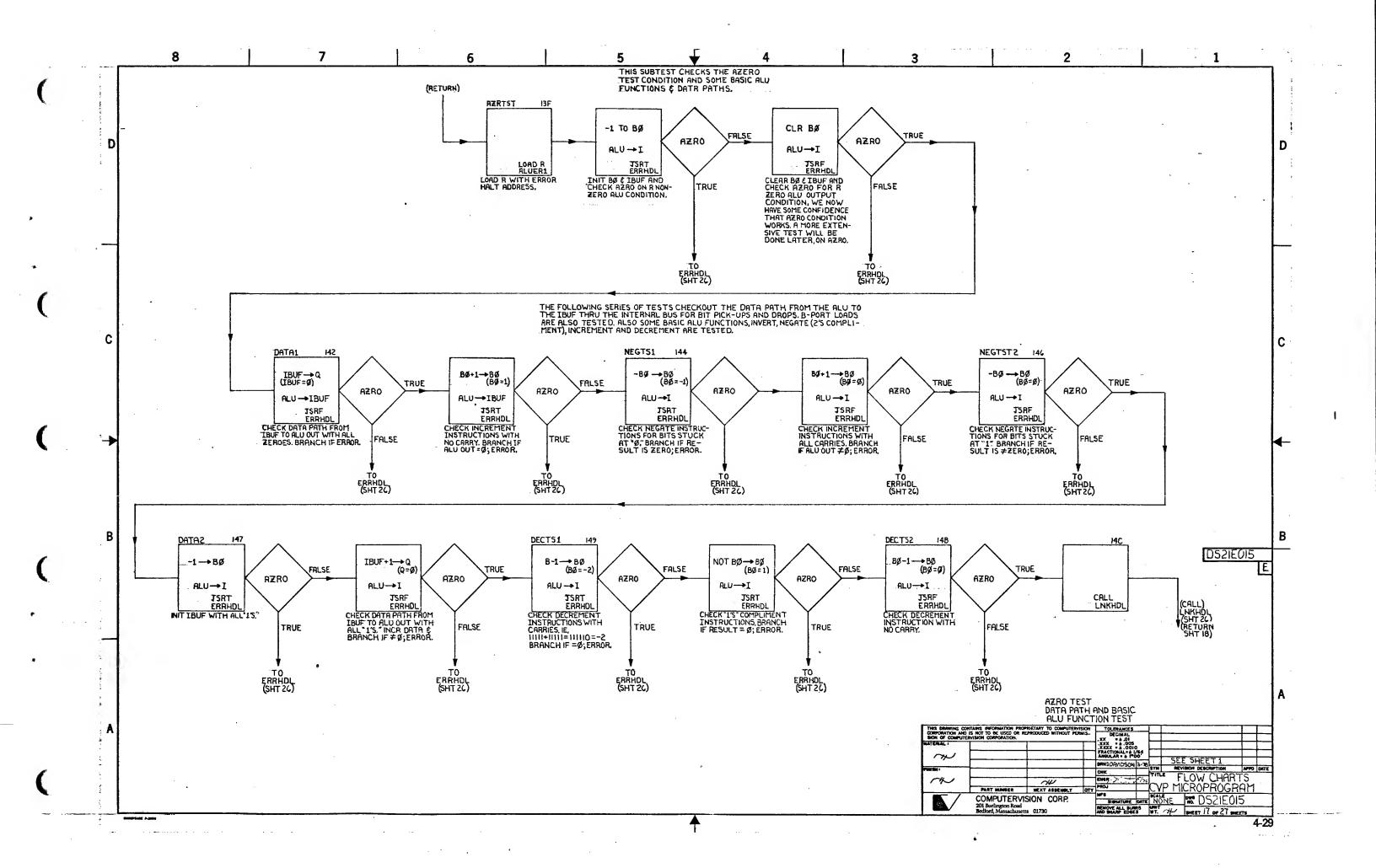


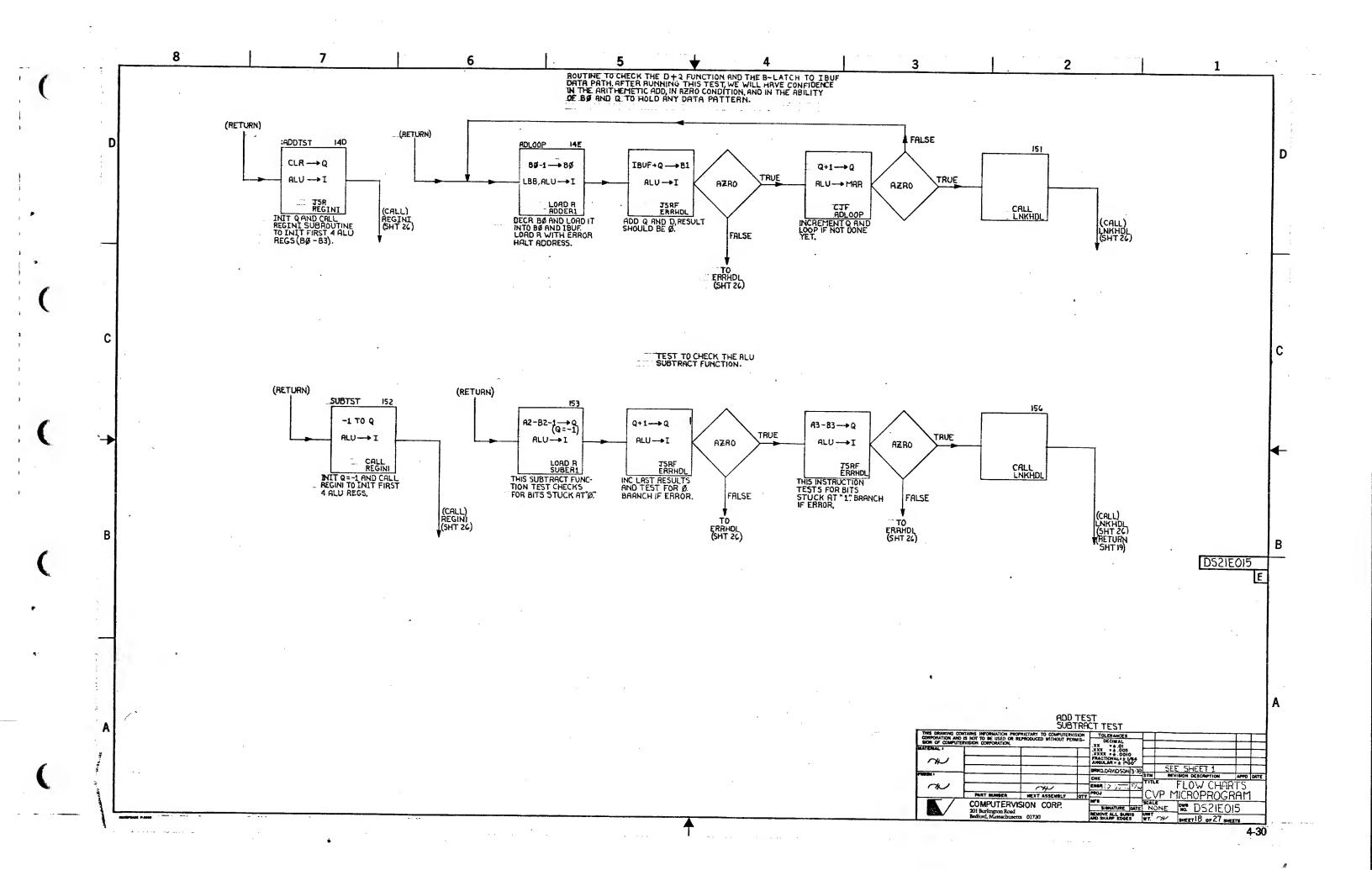


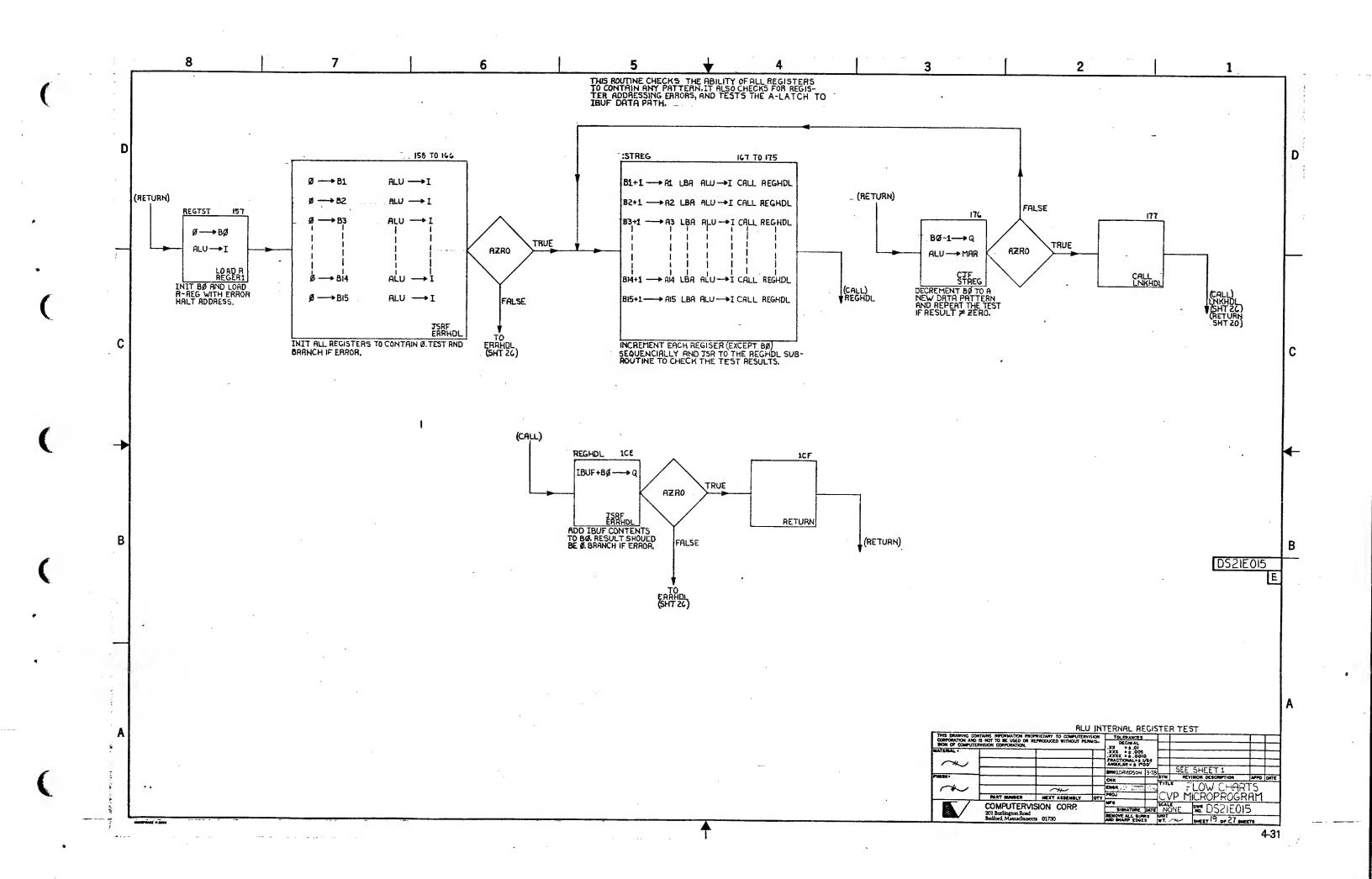


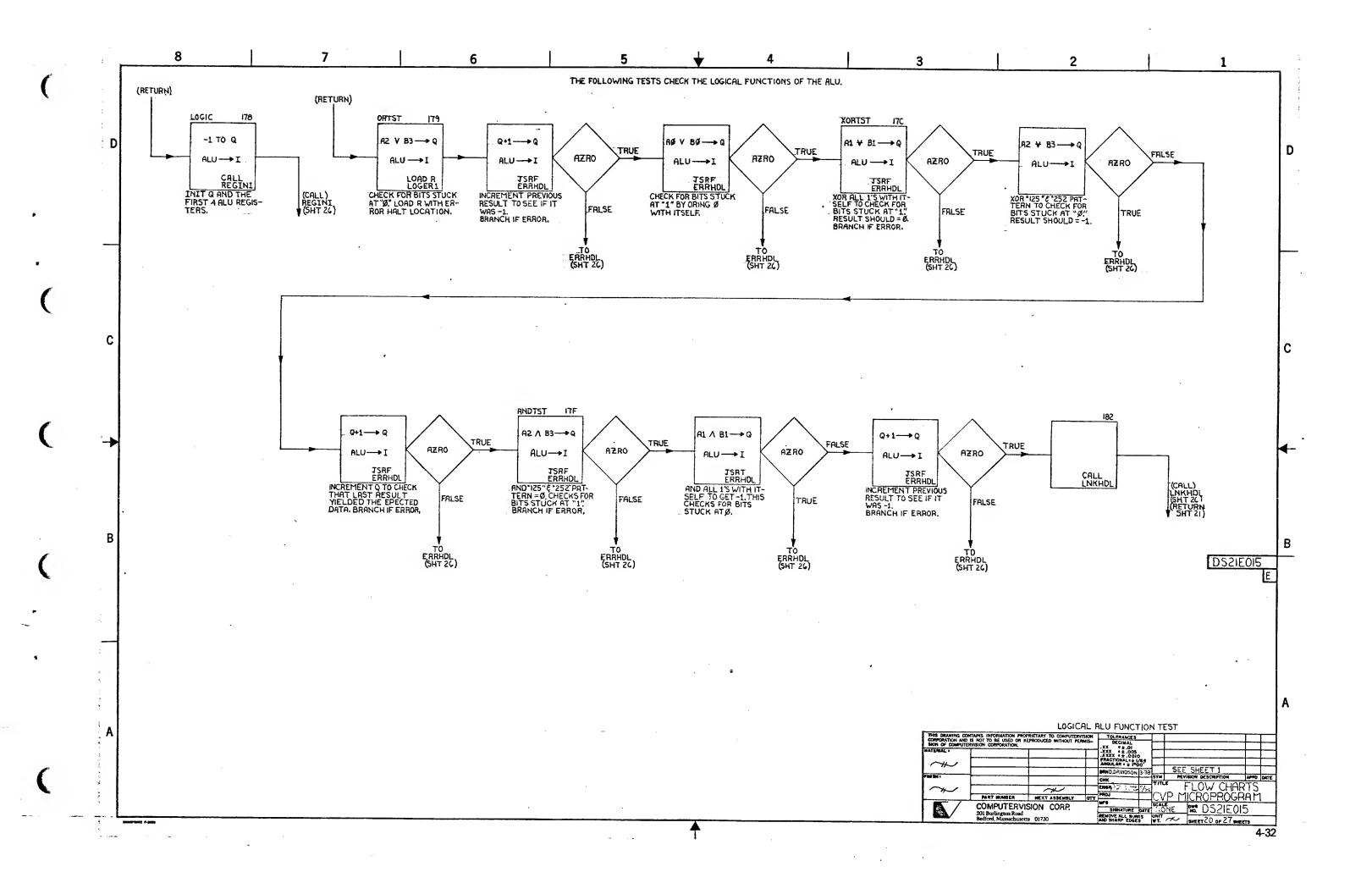


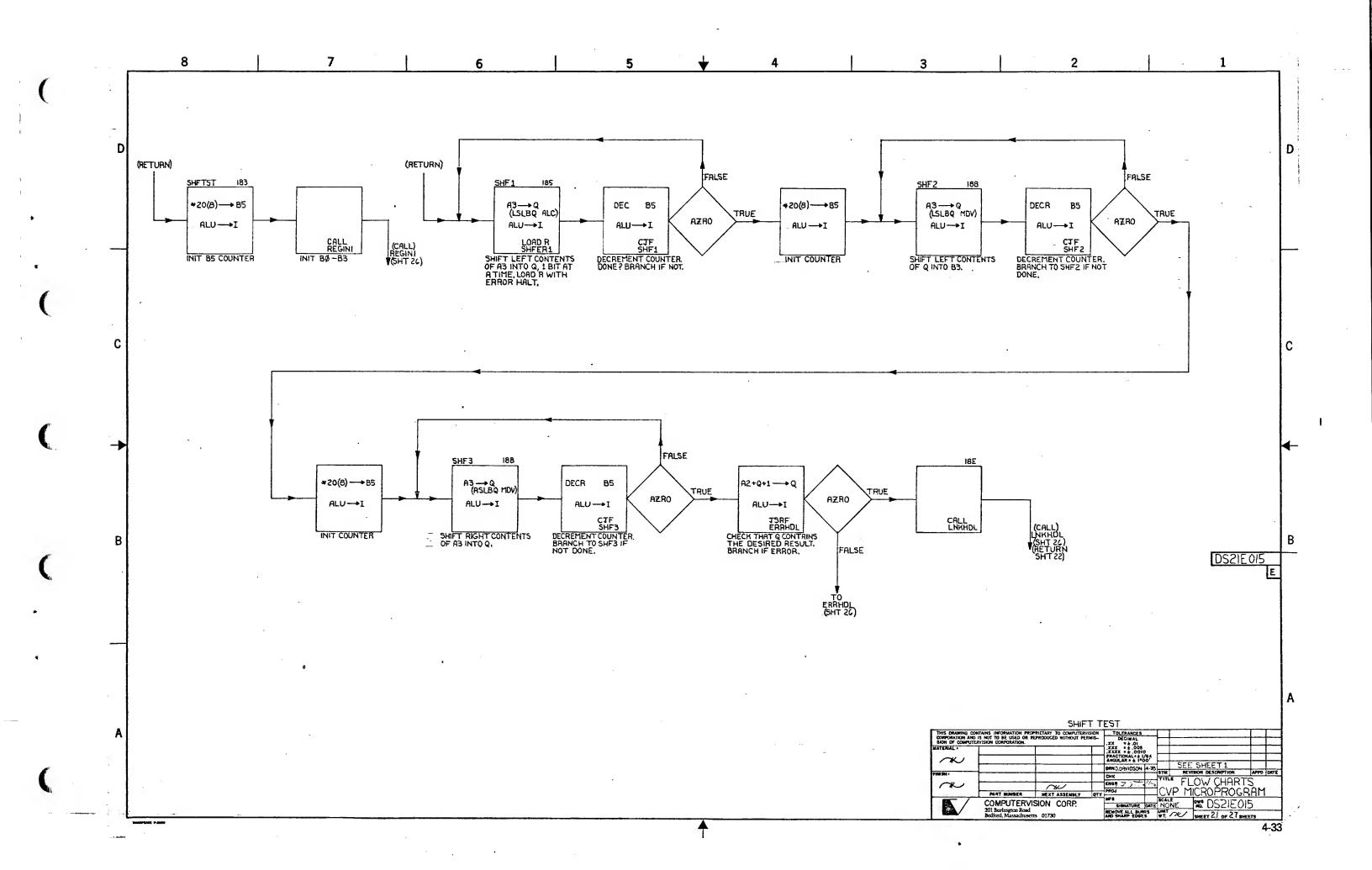


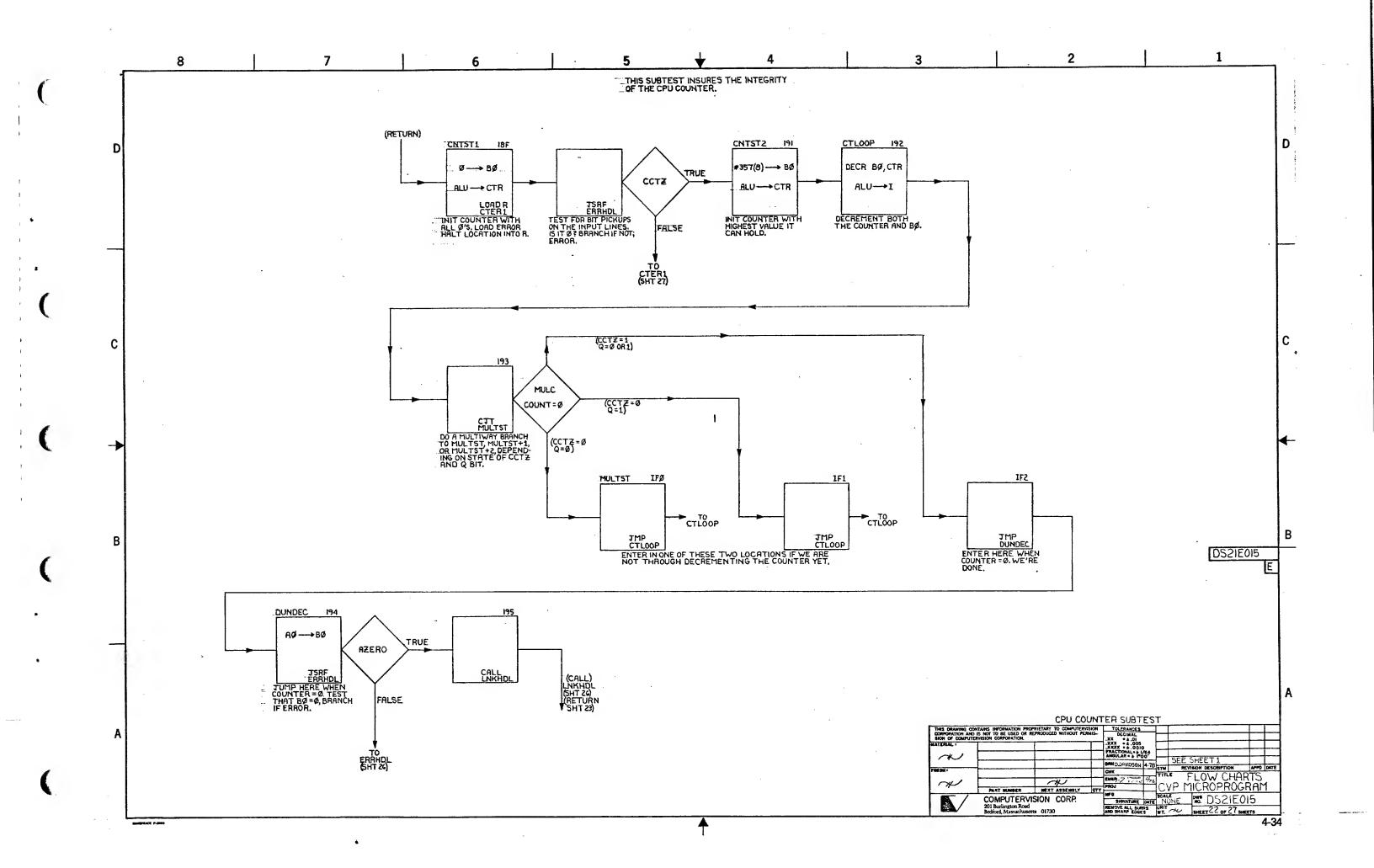


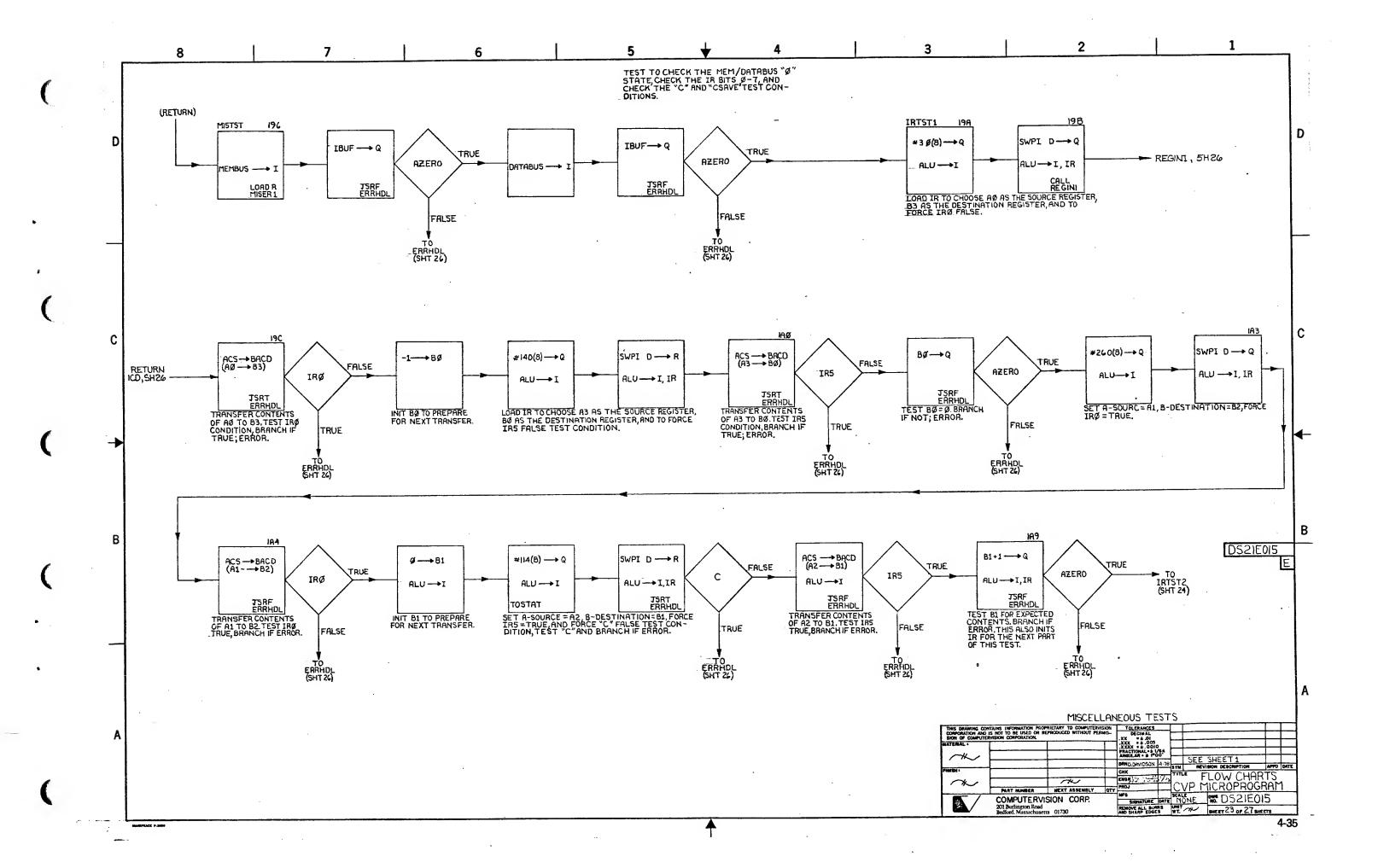


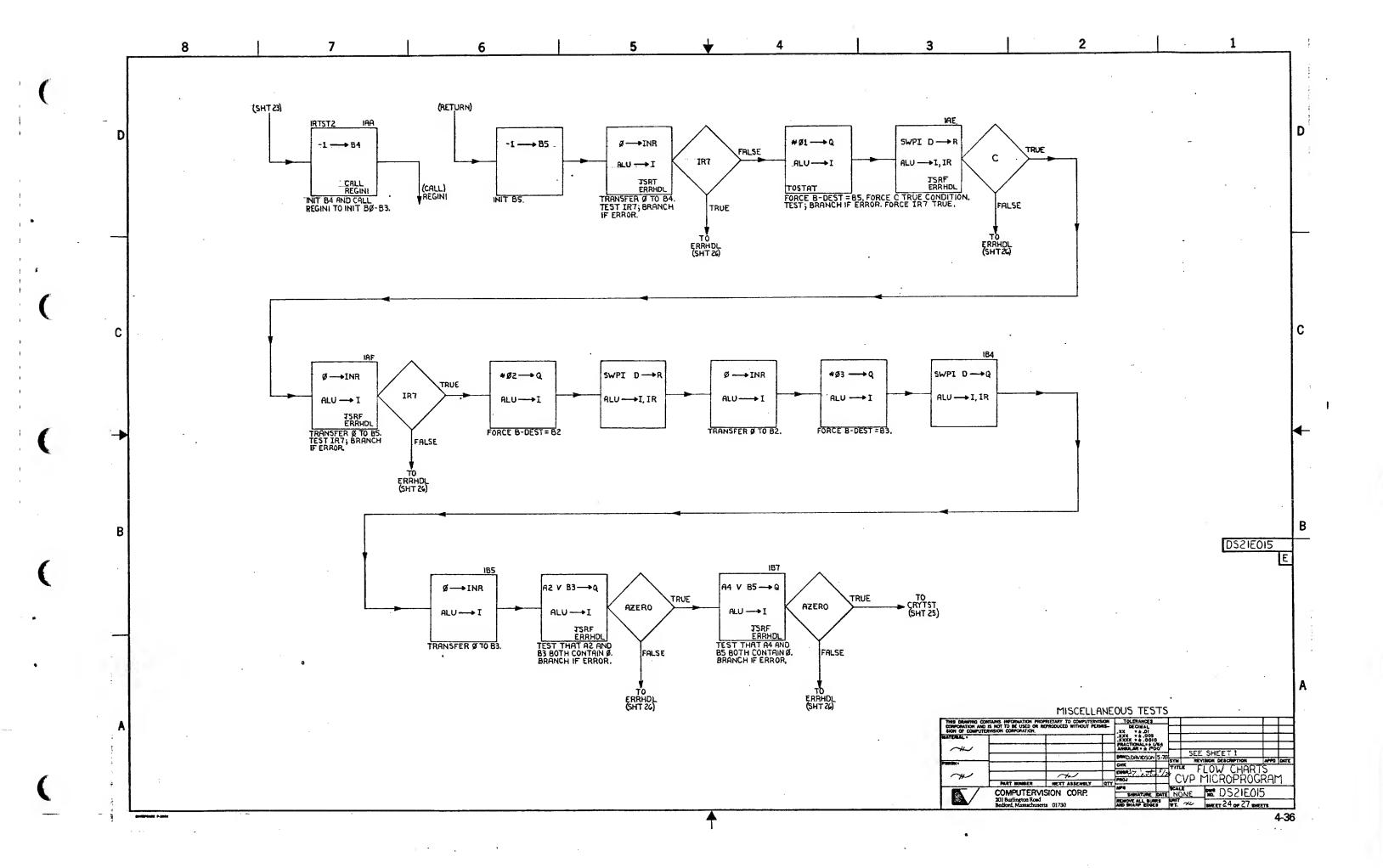


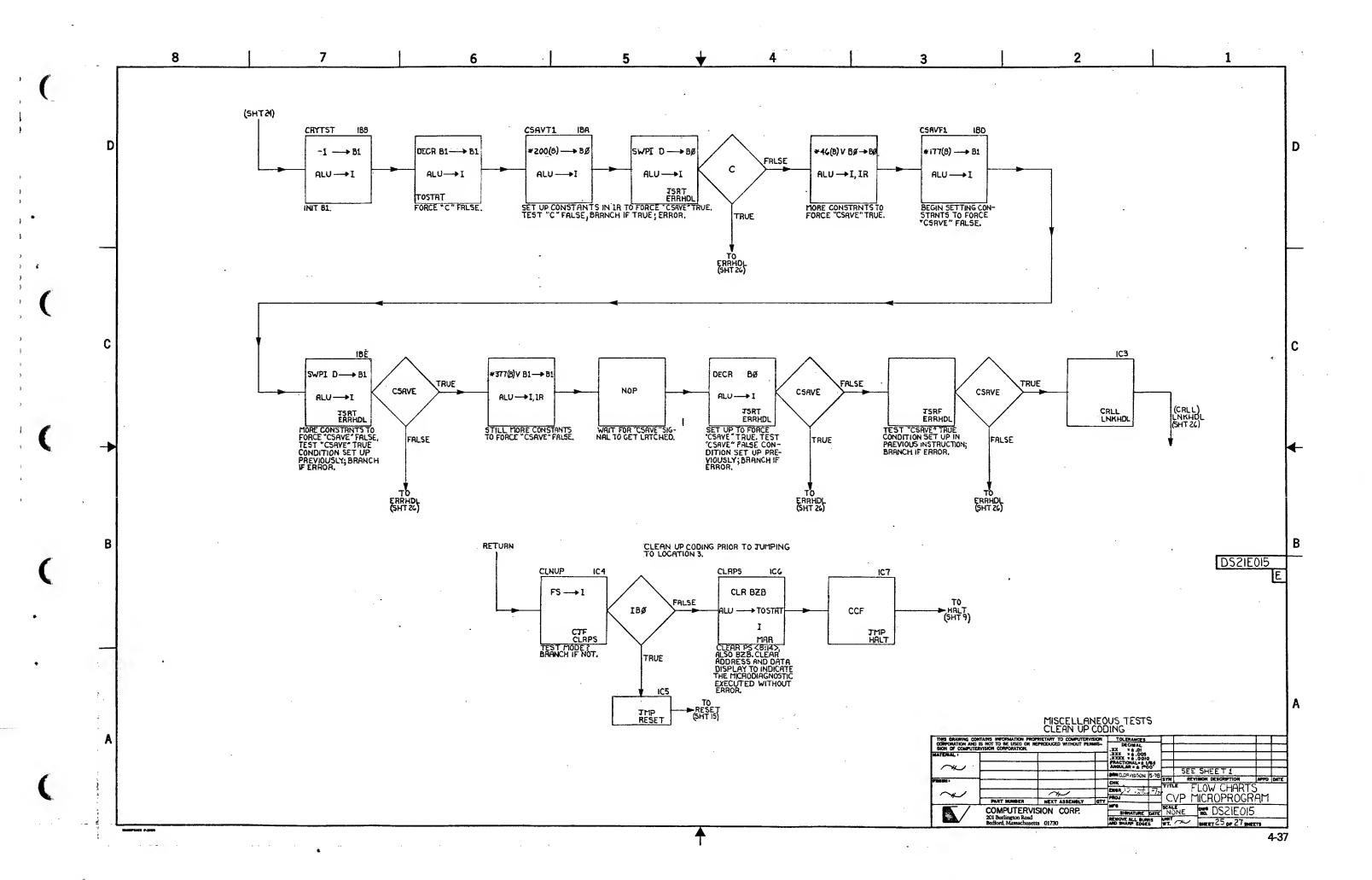


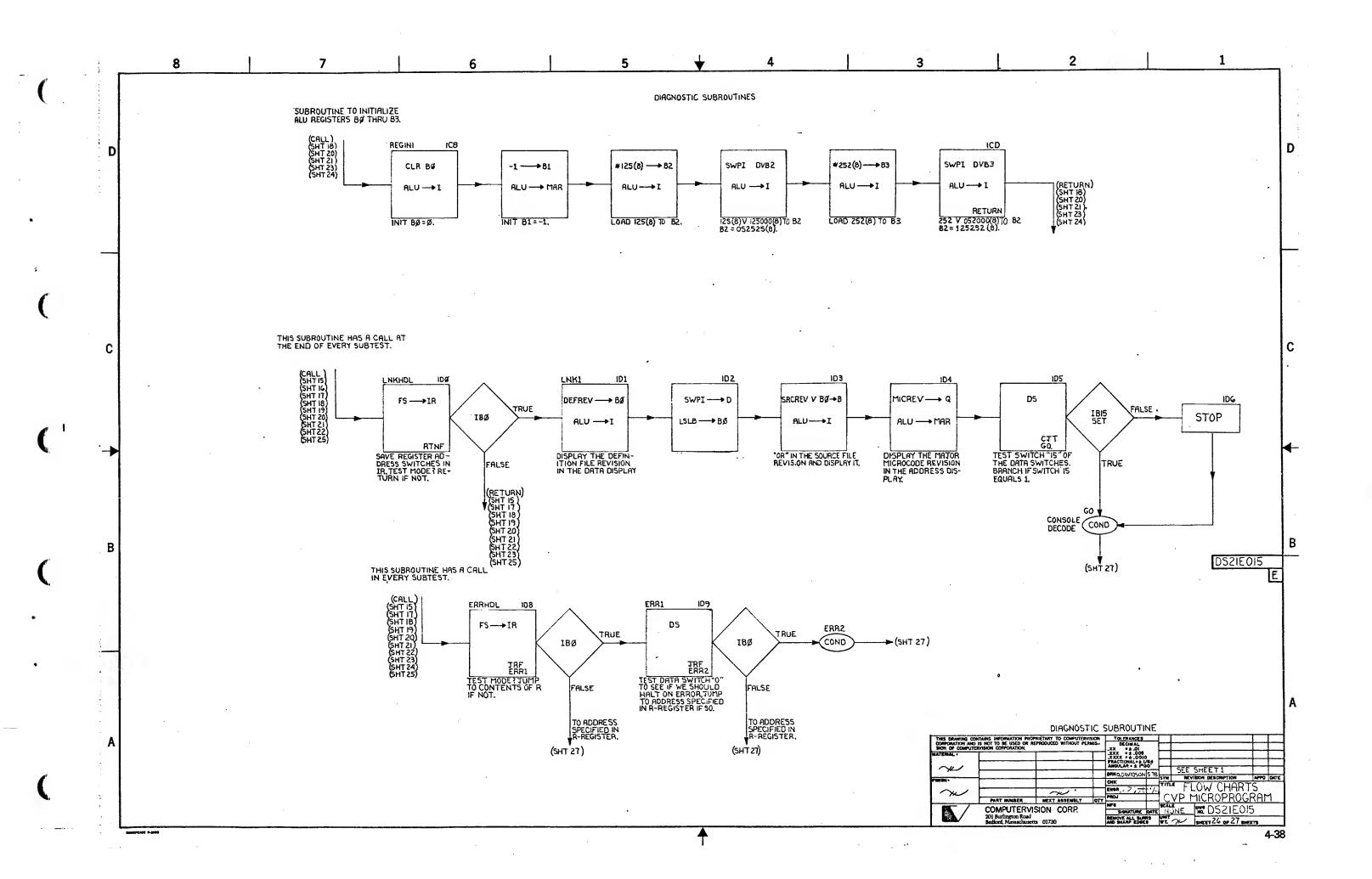


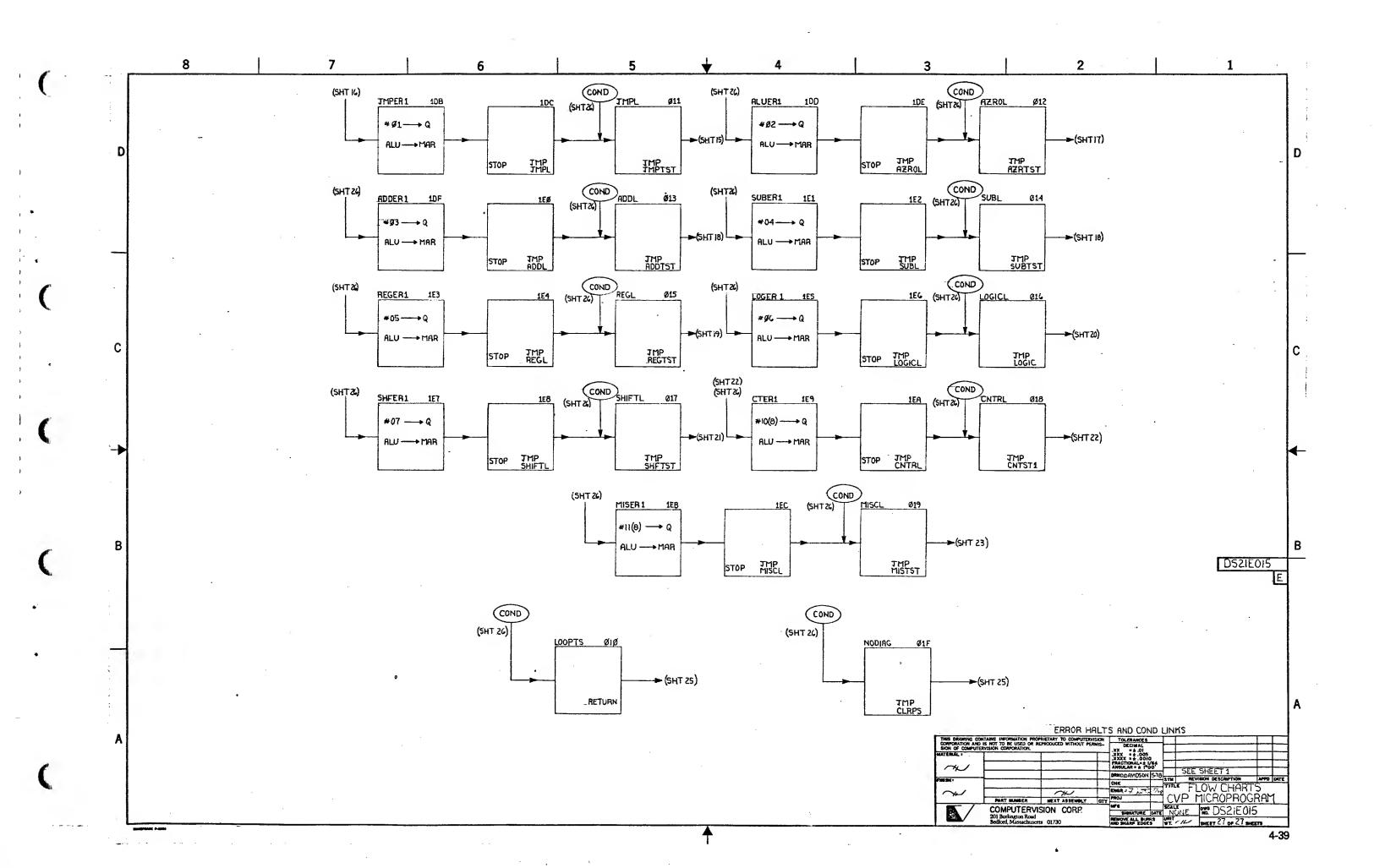






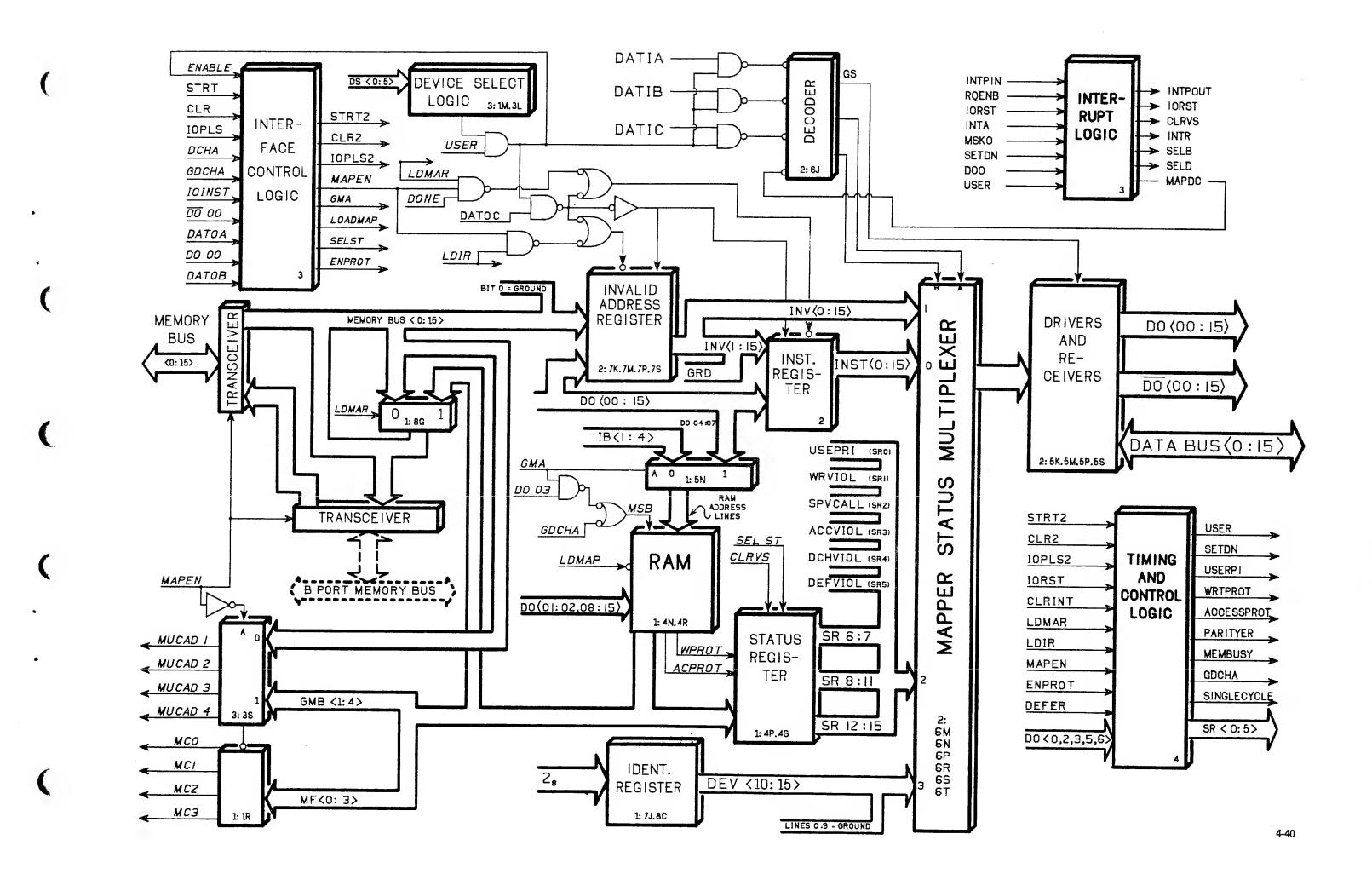


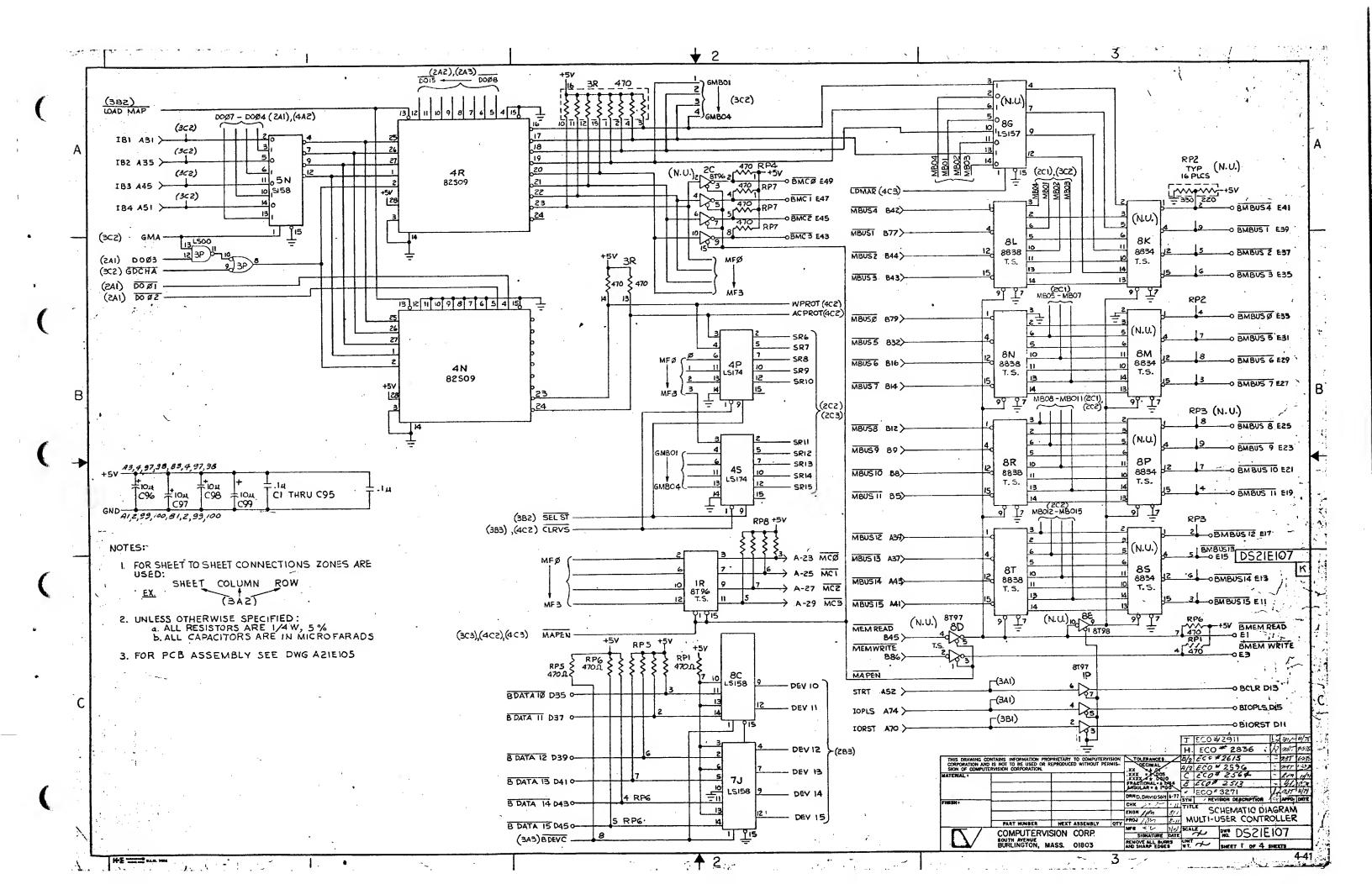


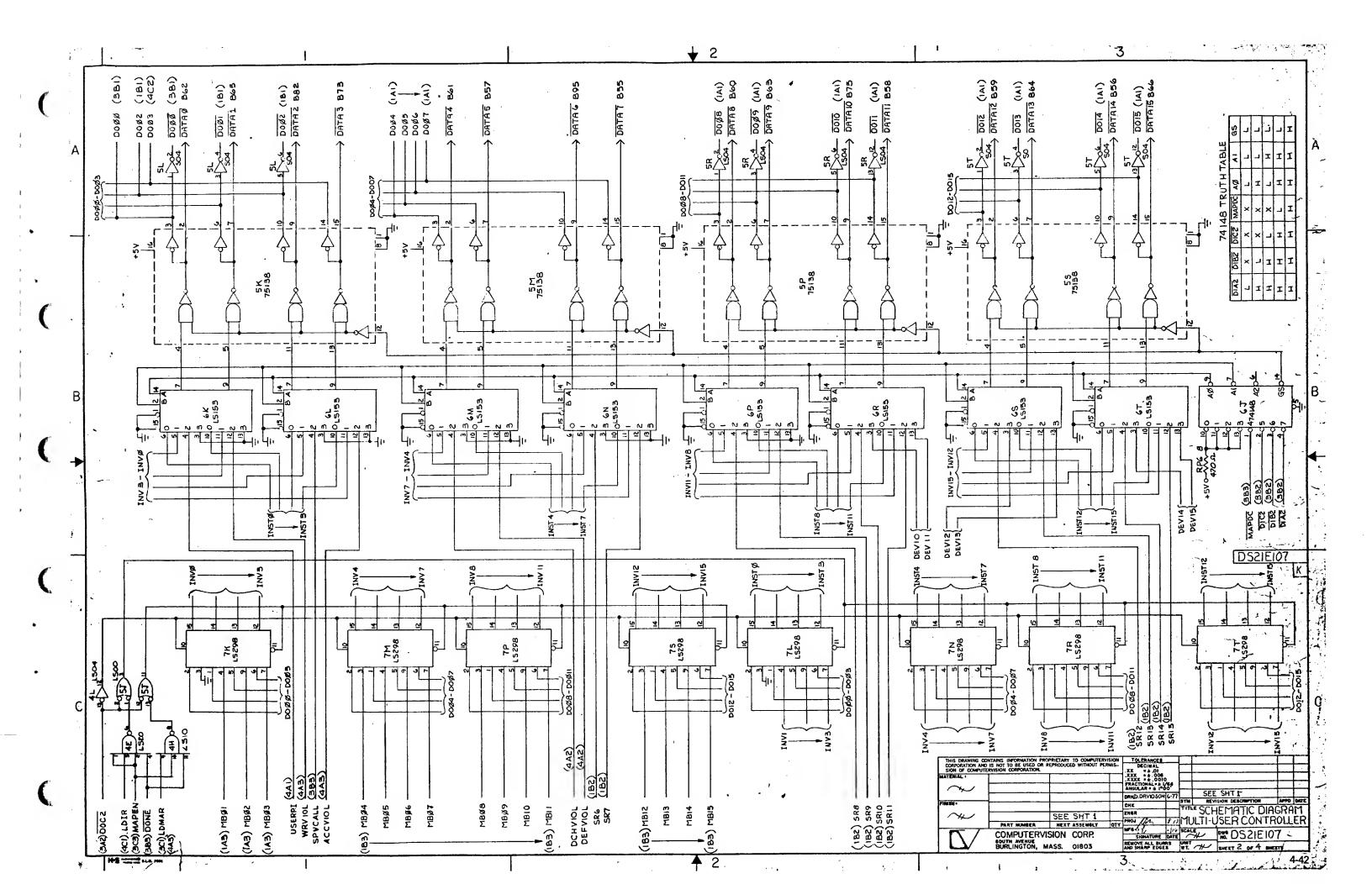


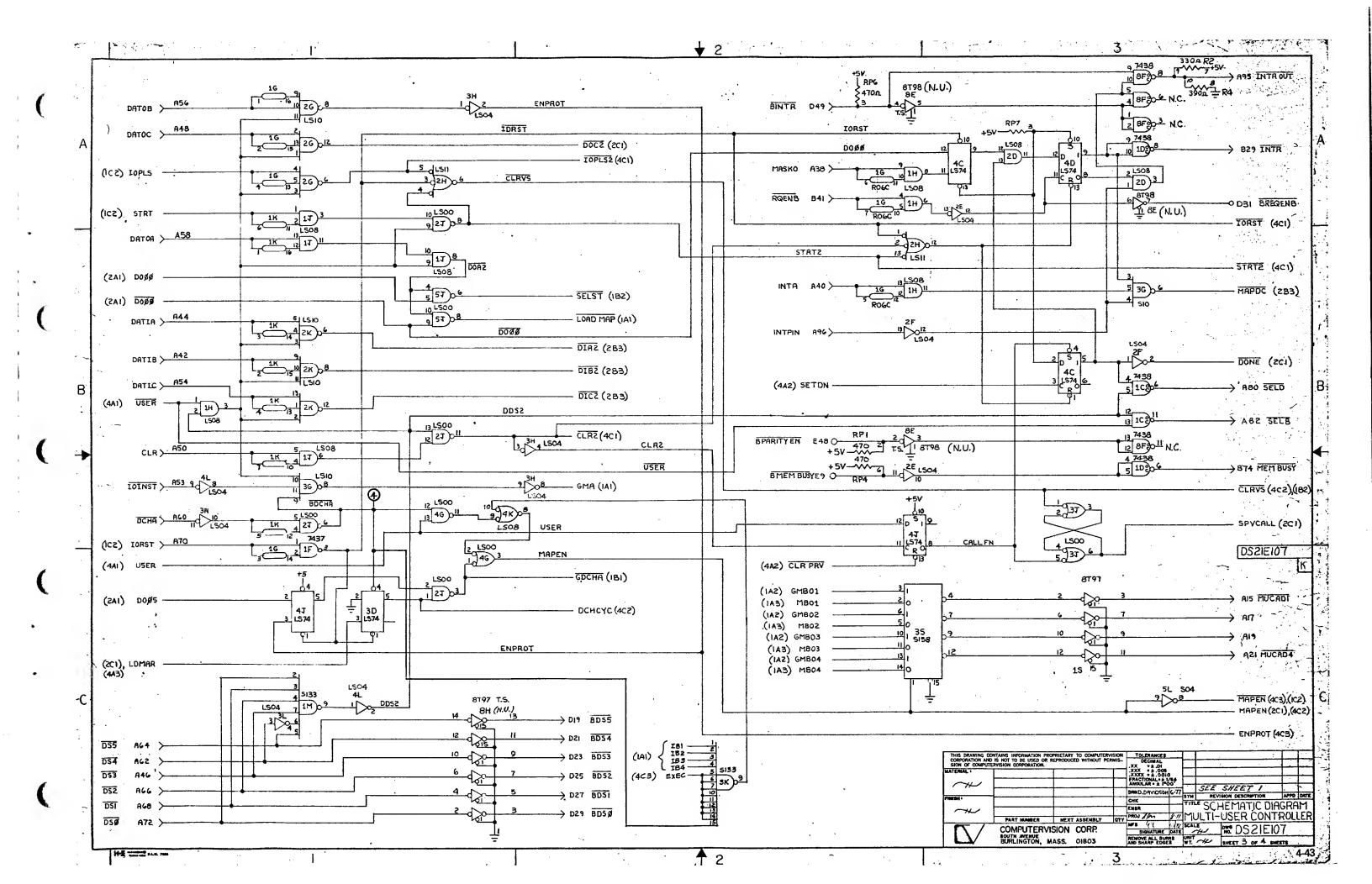
Memory Management and Protection Unit

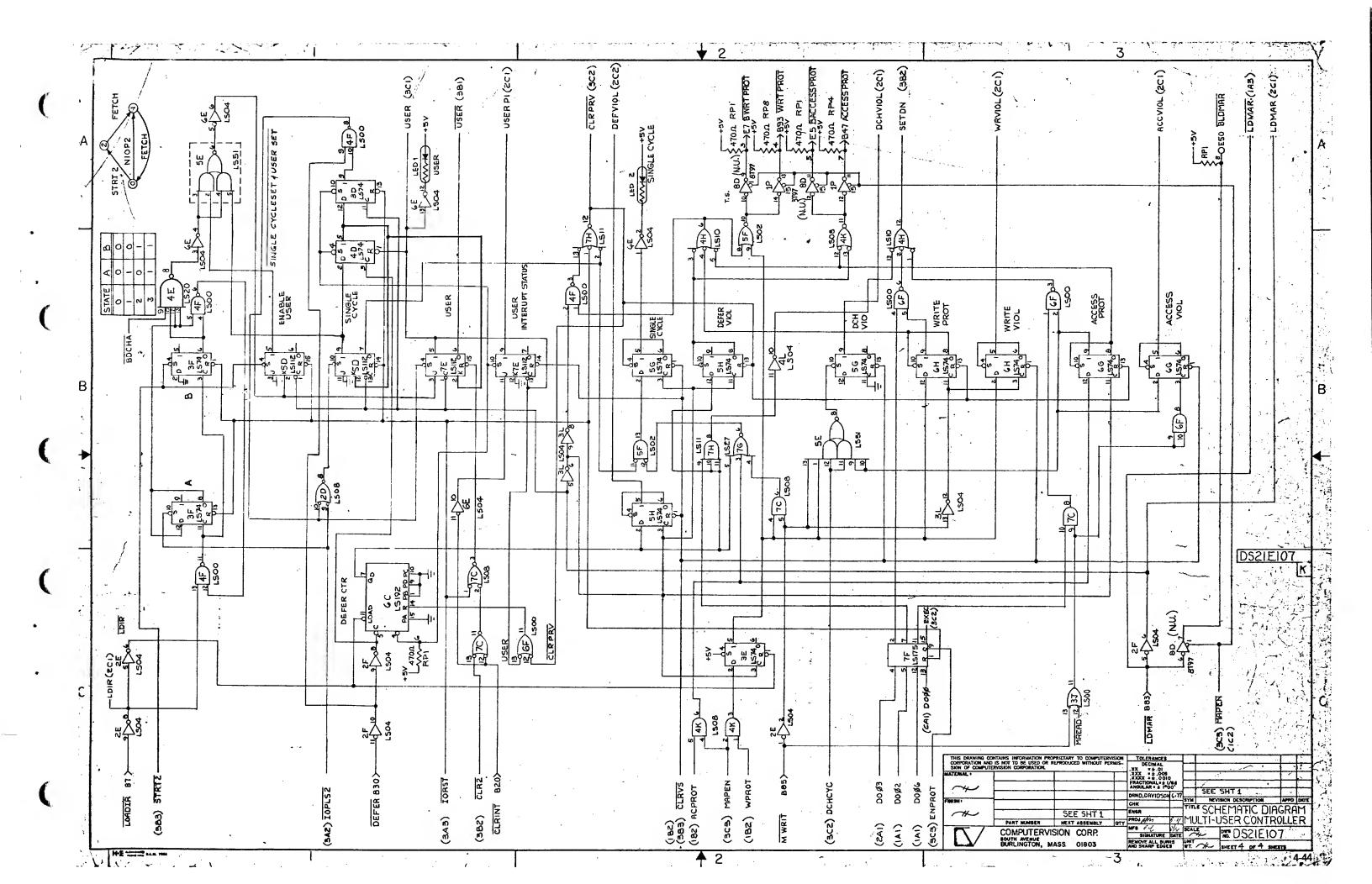
Block Diagram	4-40
Mapper RAM	4-4
Bus Logic	4-4
Mapper Status	4-42
I/O Logic	4-43
Timing Logic	4-44
Protection Logic	4-44





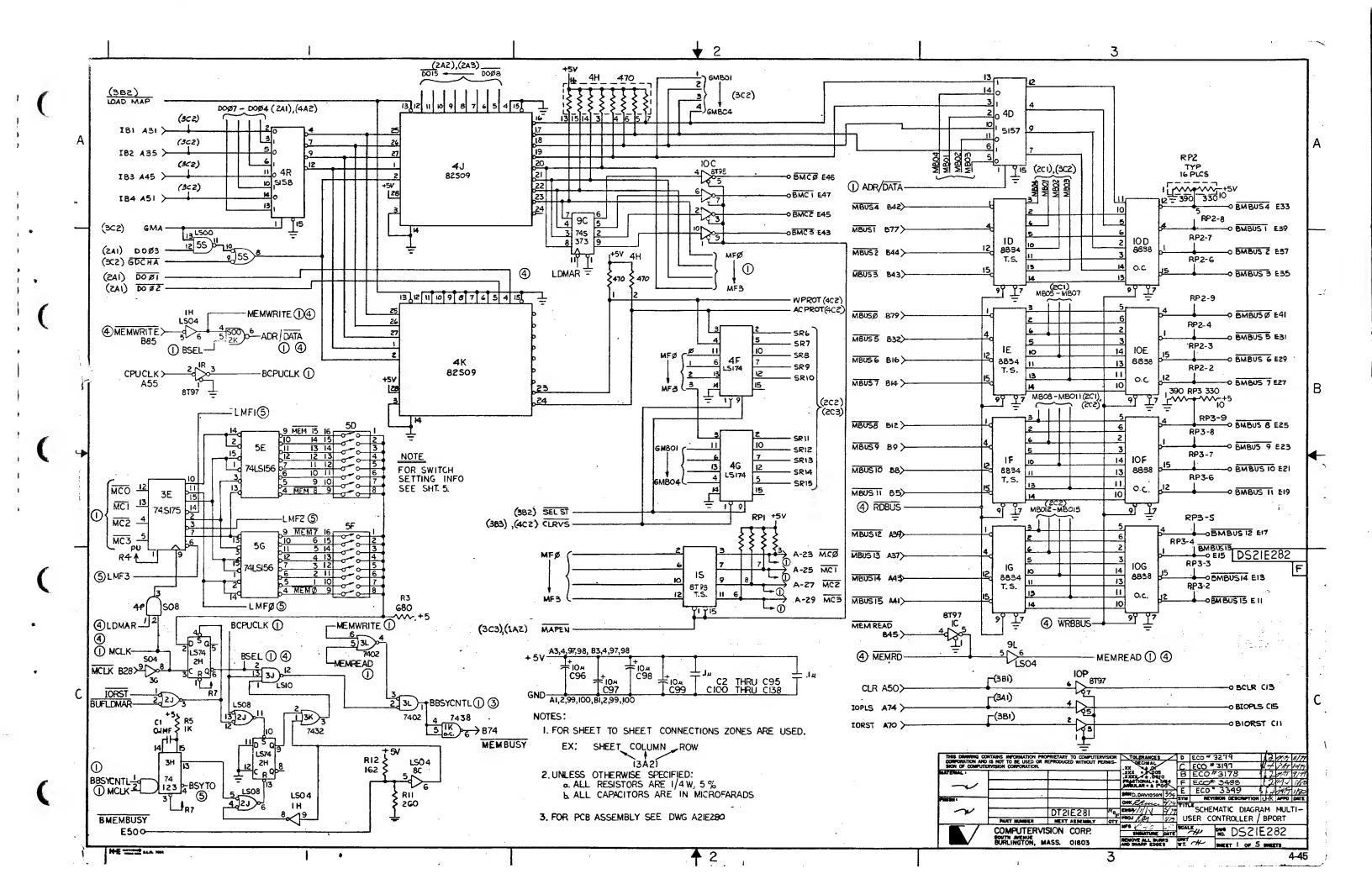


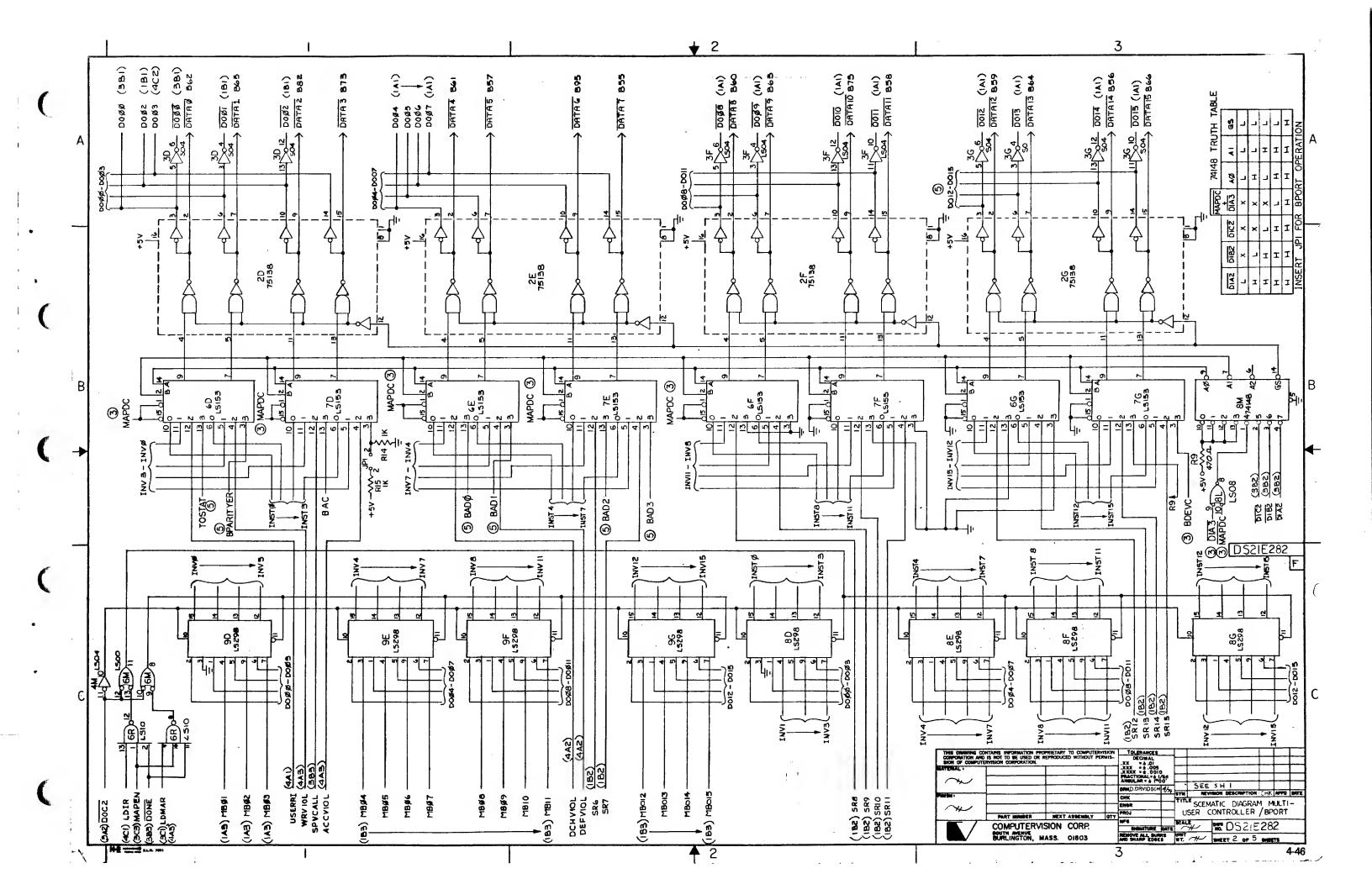


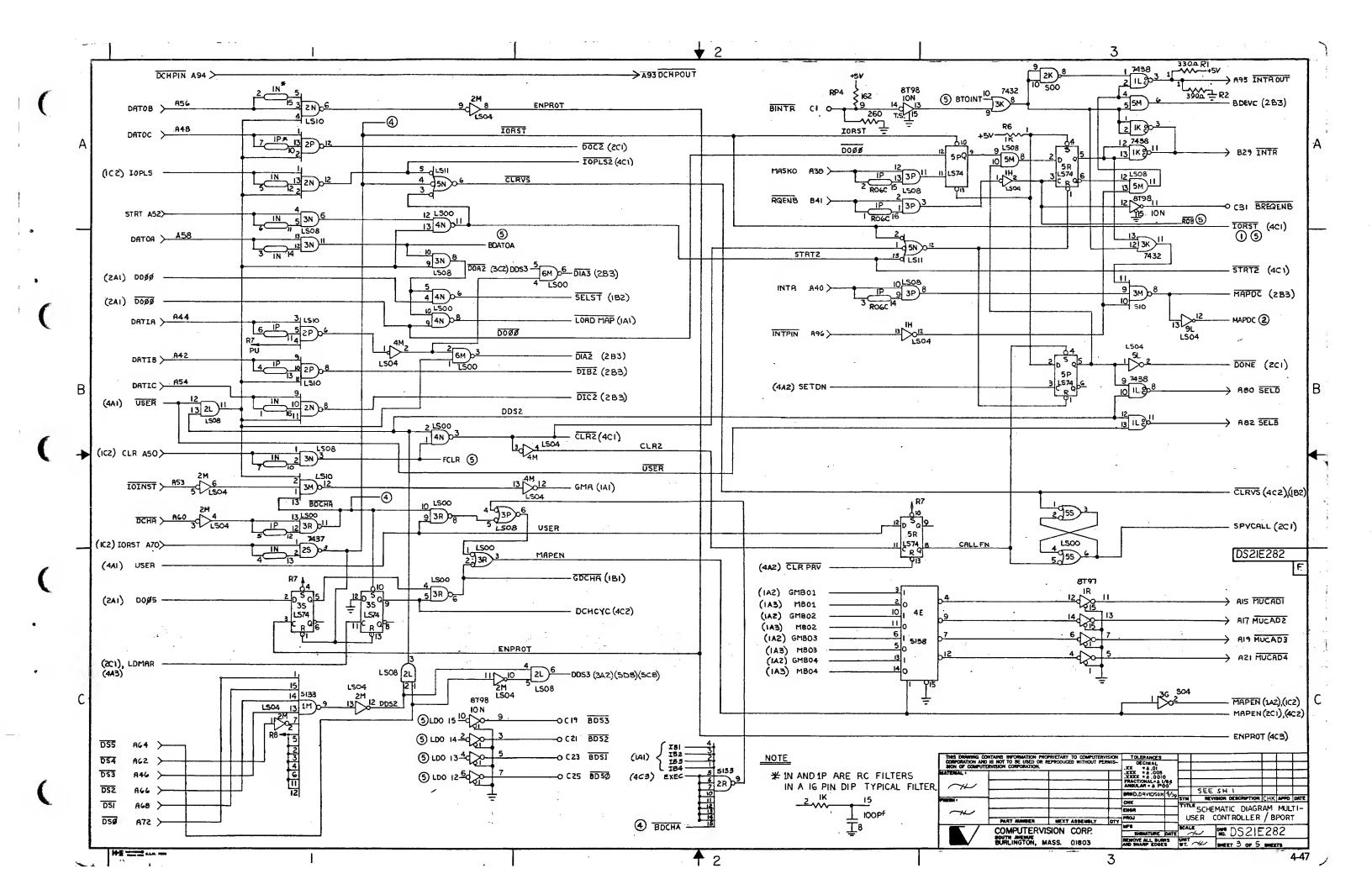


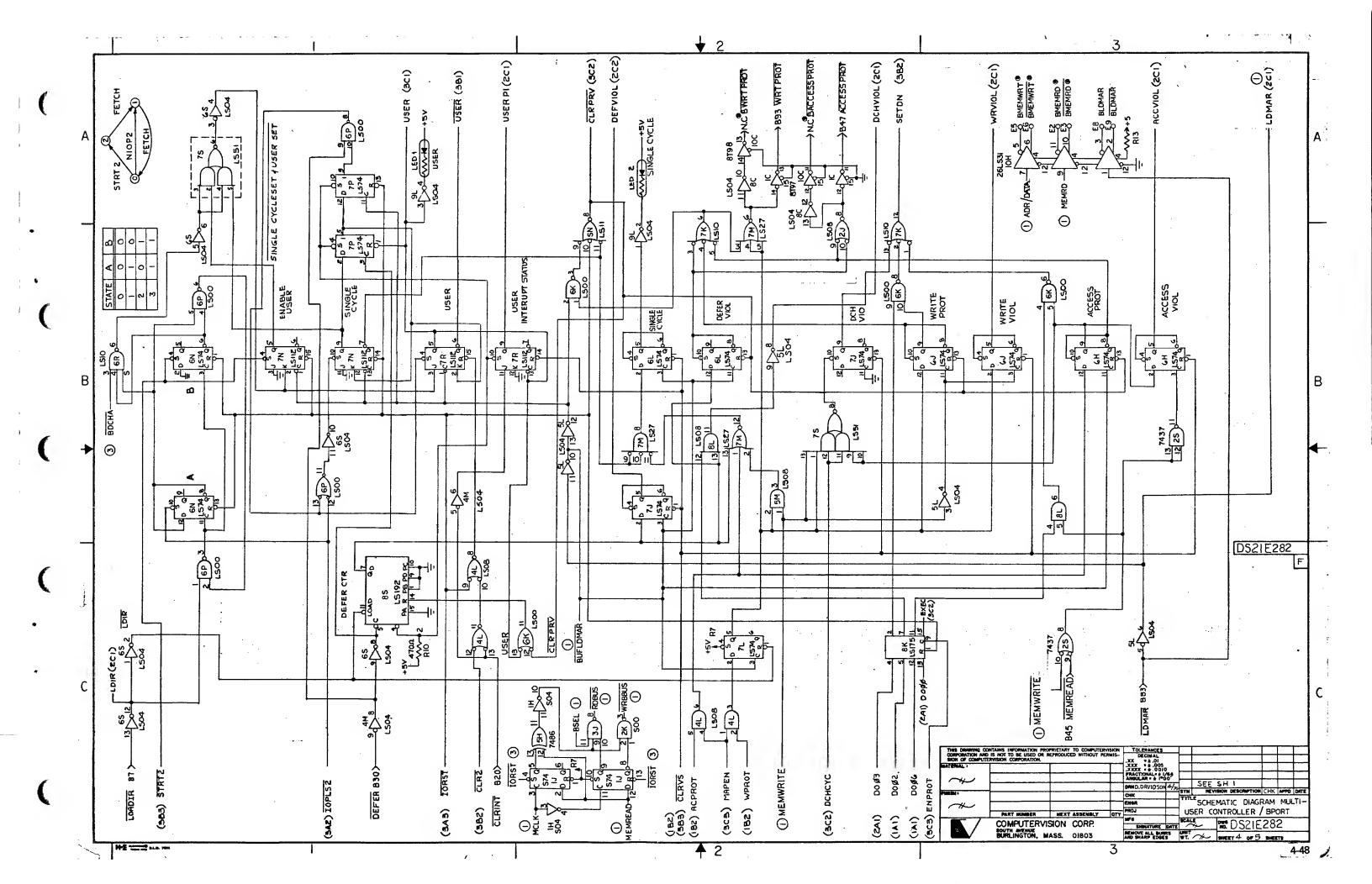
B-Port Memory Managment and Protection Unit

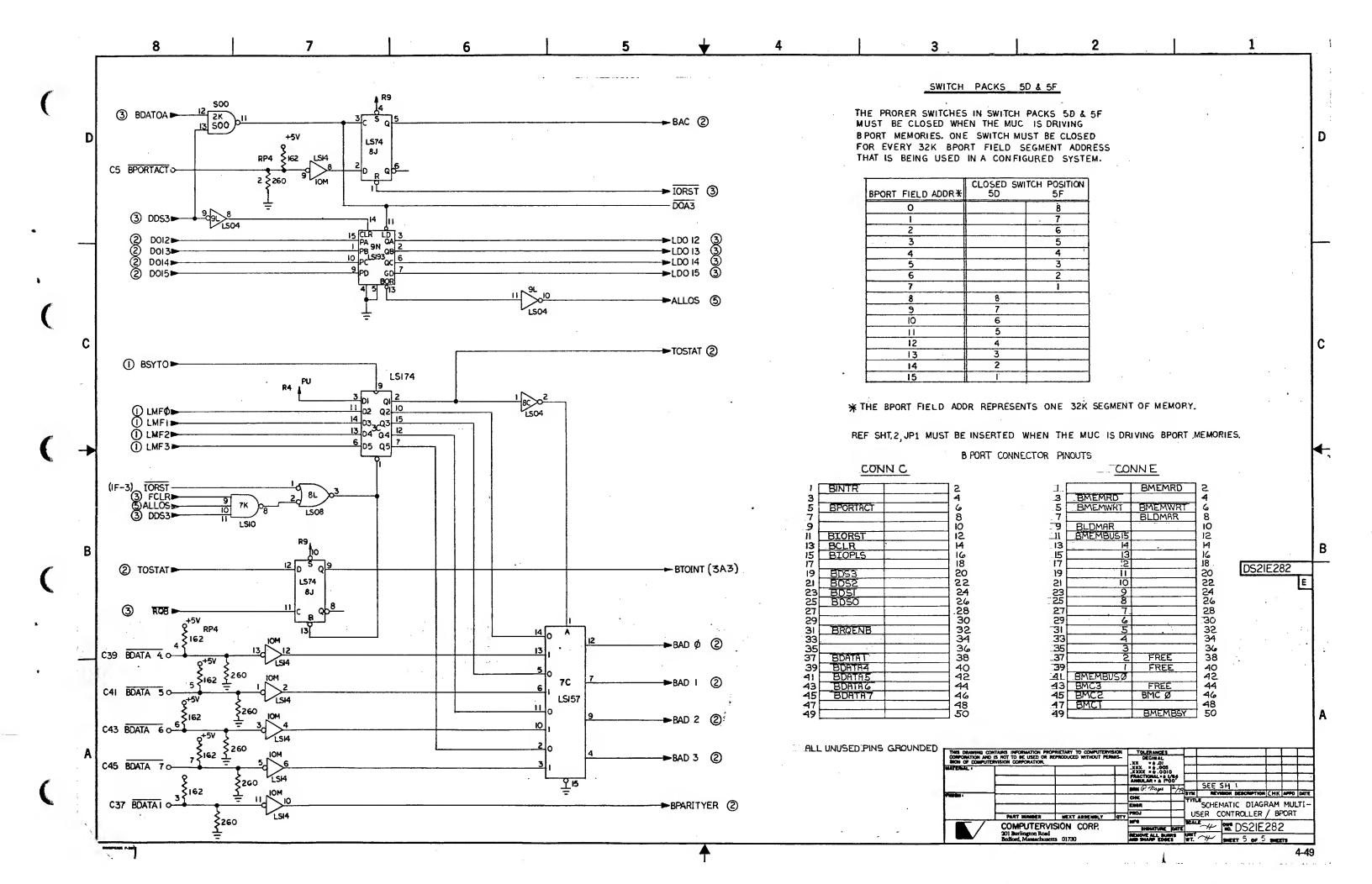
Mapper Ram	4-45
Bus Logic	4-45
Mapper Status Logic	4-46
I/O Logic	4-47
Timing Logic	4-48
Protection Logic	4-48
Switch Settings	4-49
Jumper Configuration	4-49
B-Port Connector Pinouts	4-49



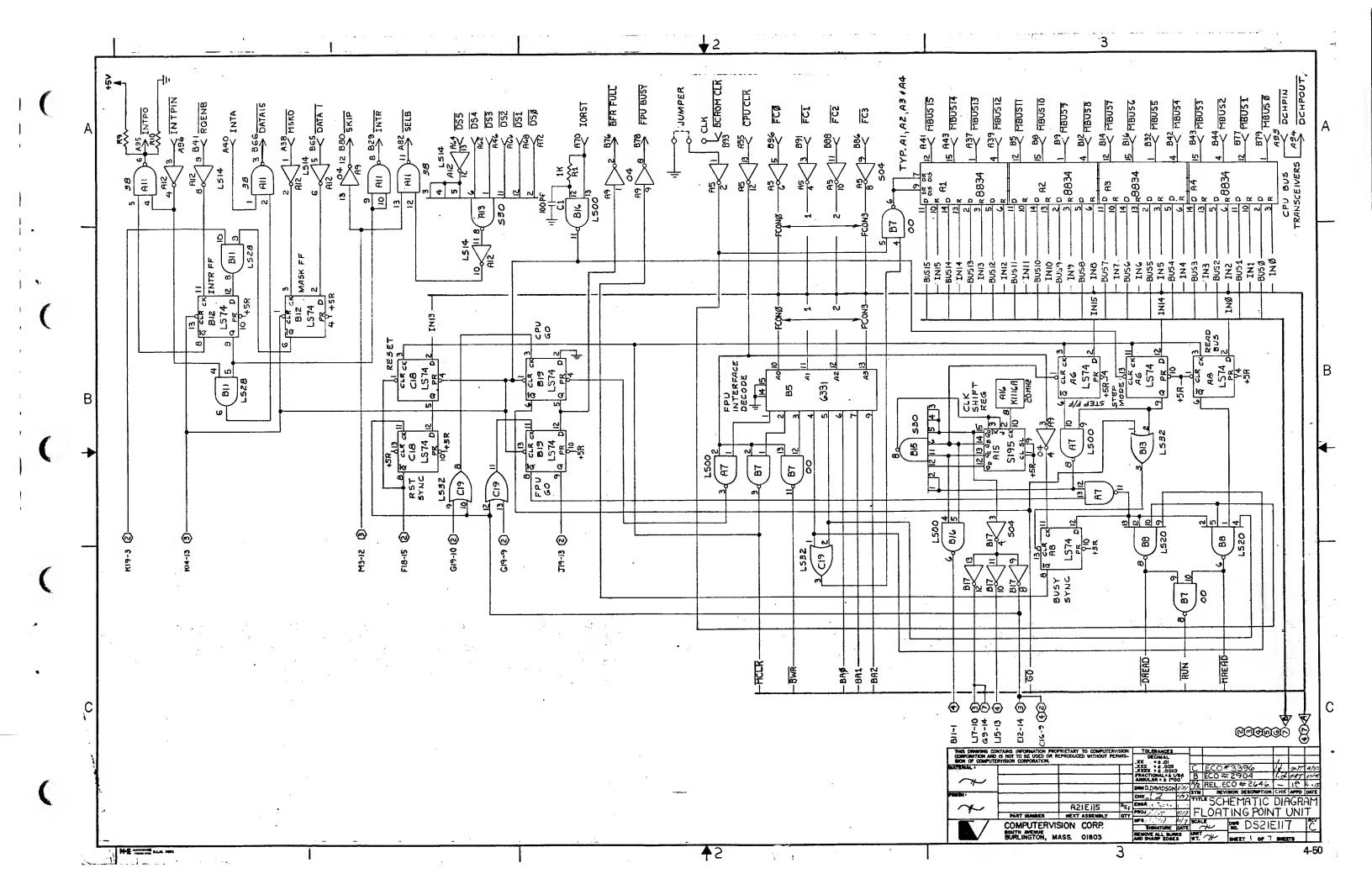


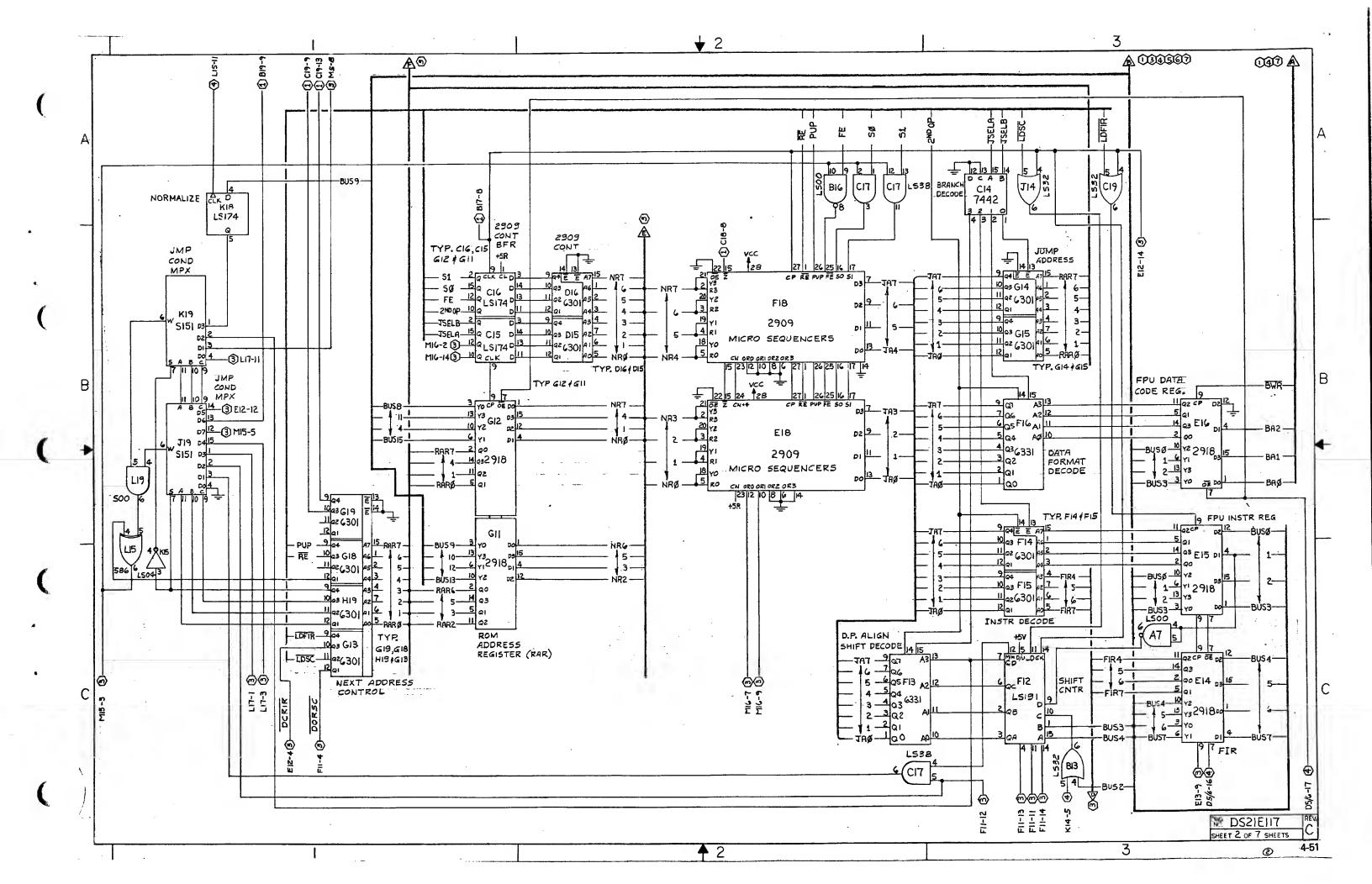


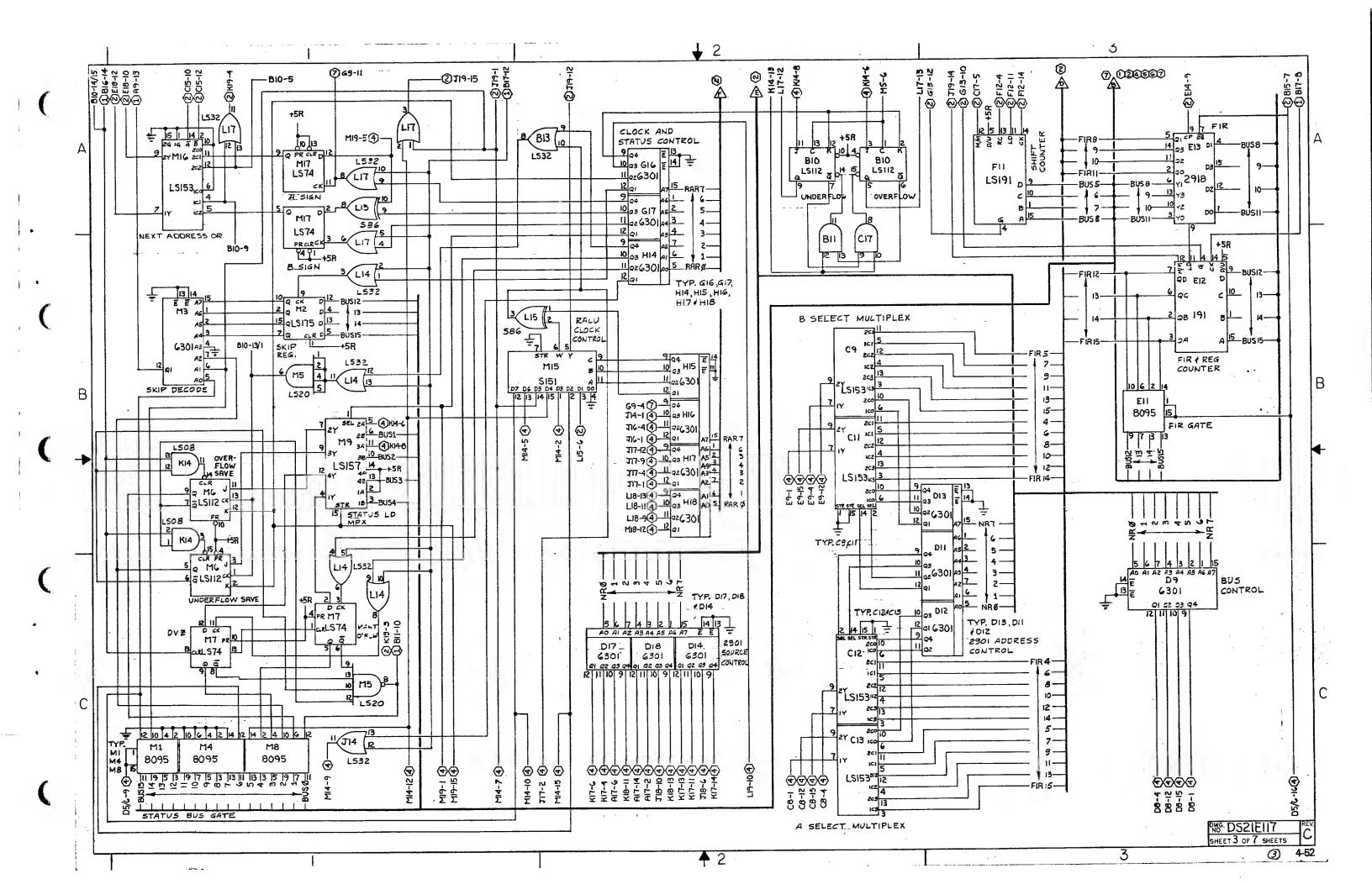


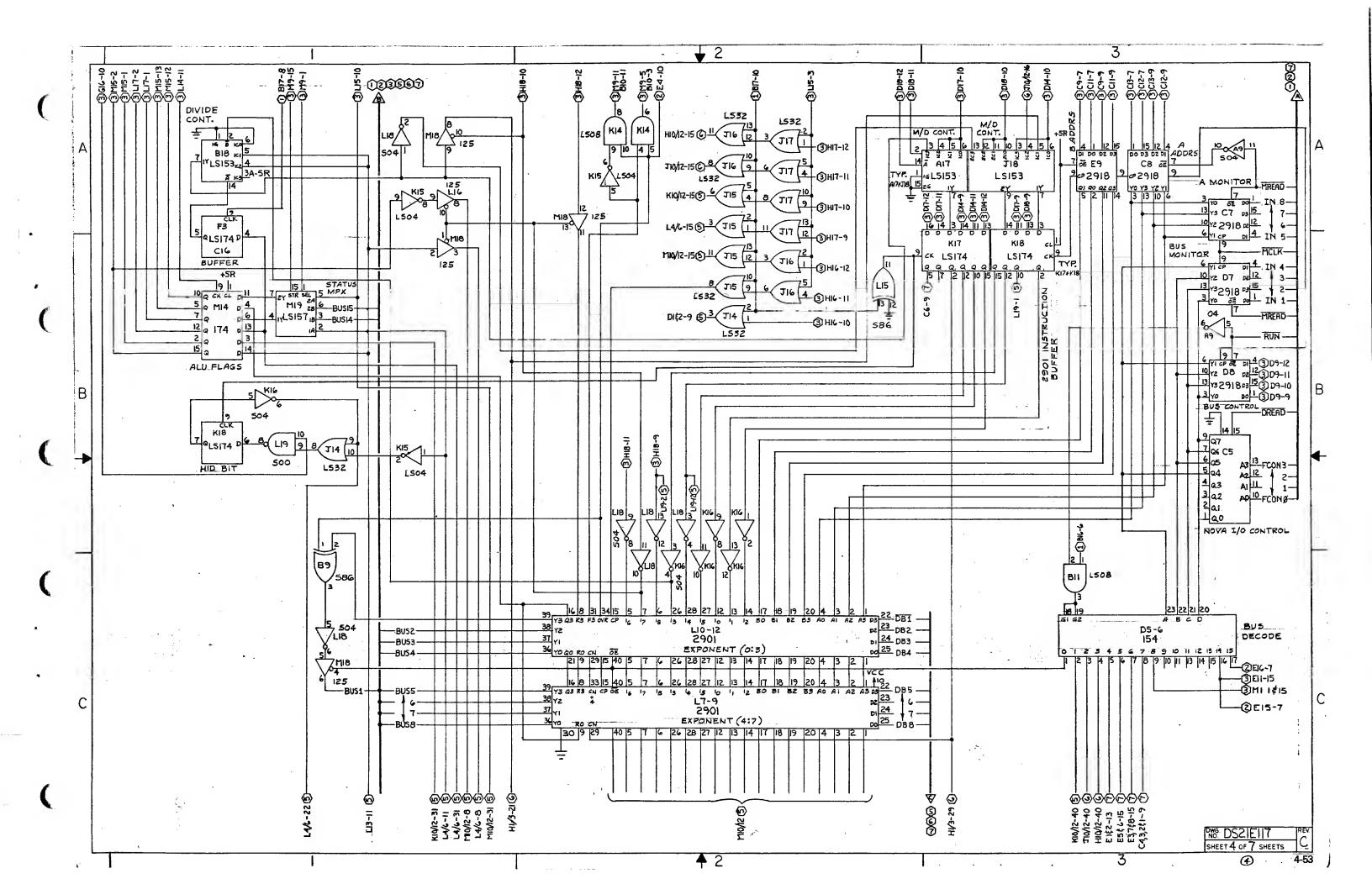


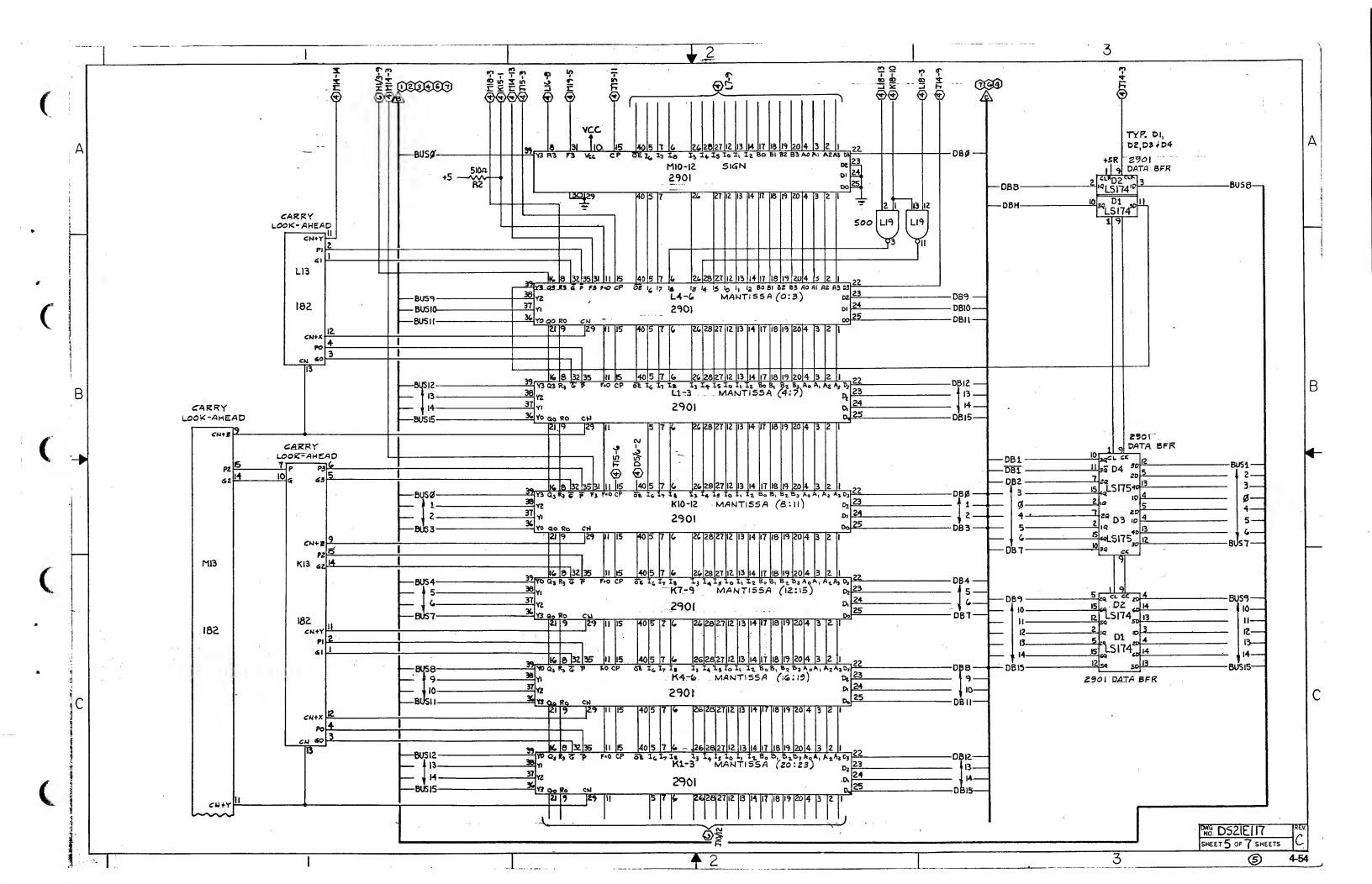
Floating Point Unit

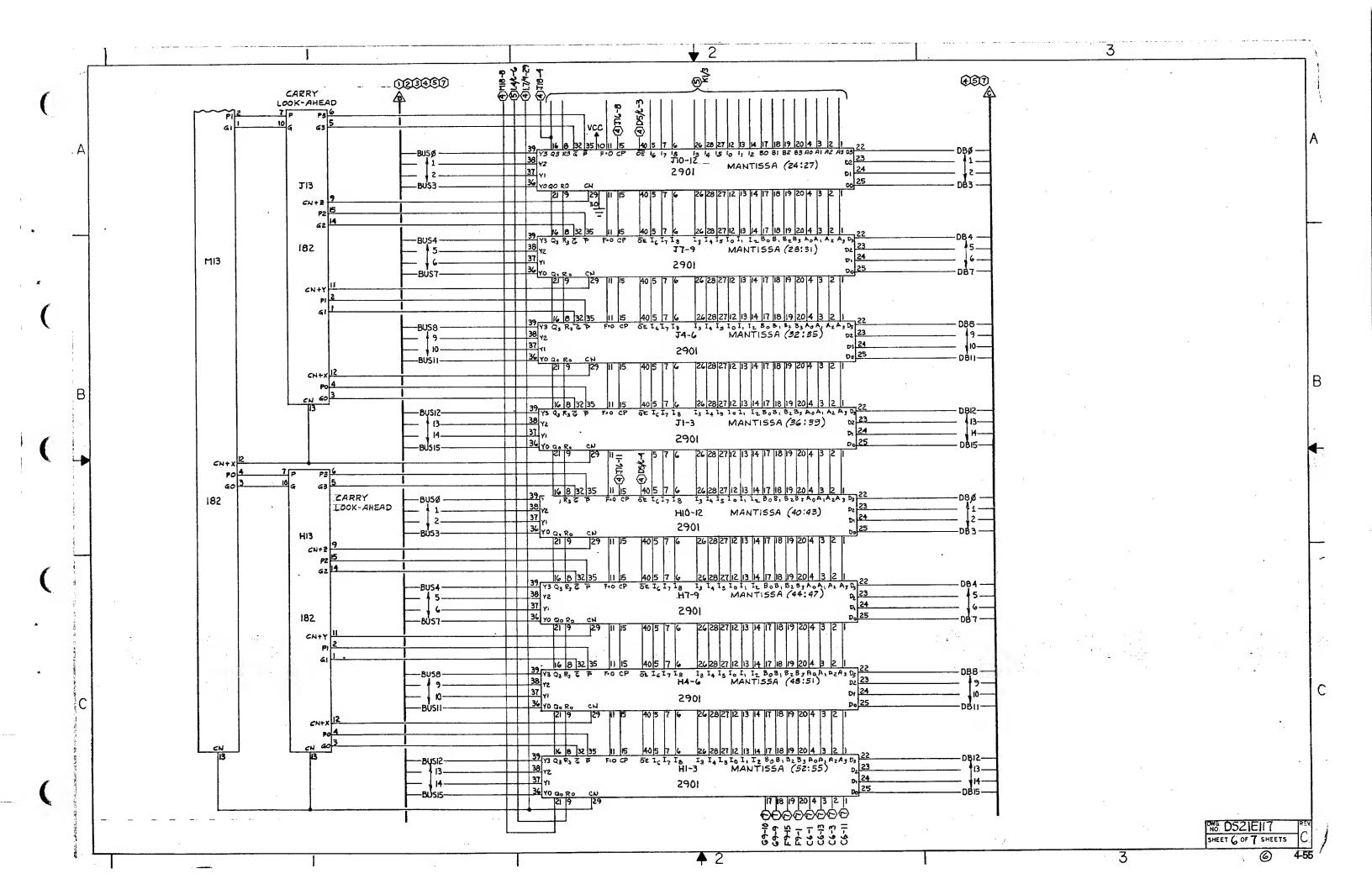


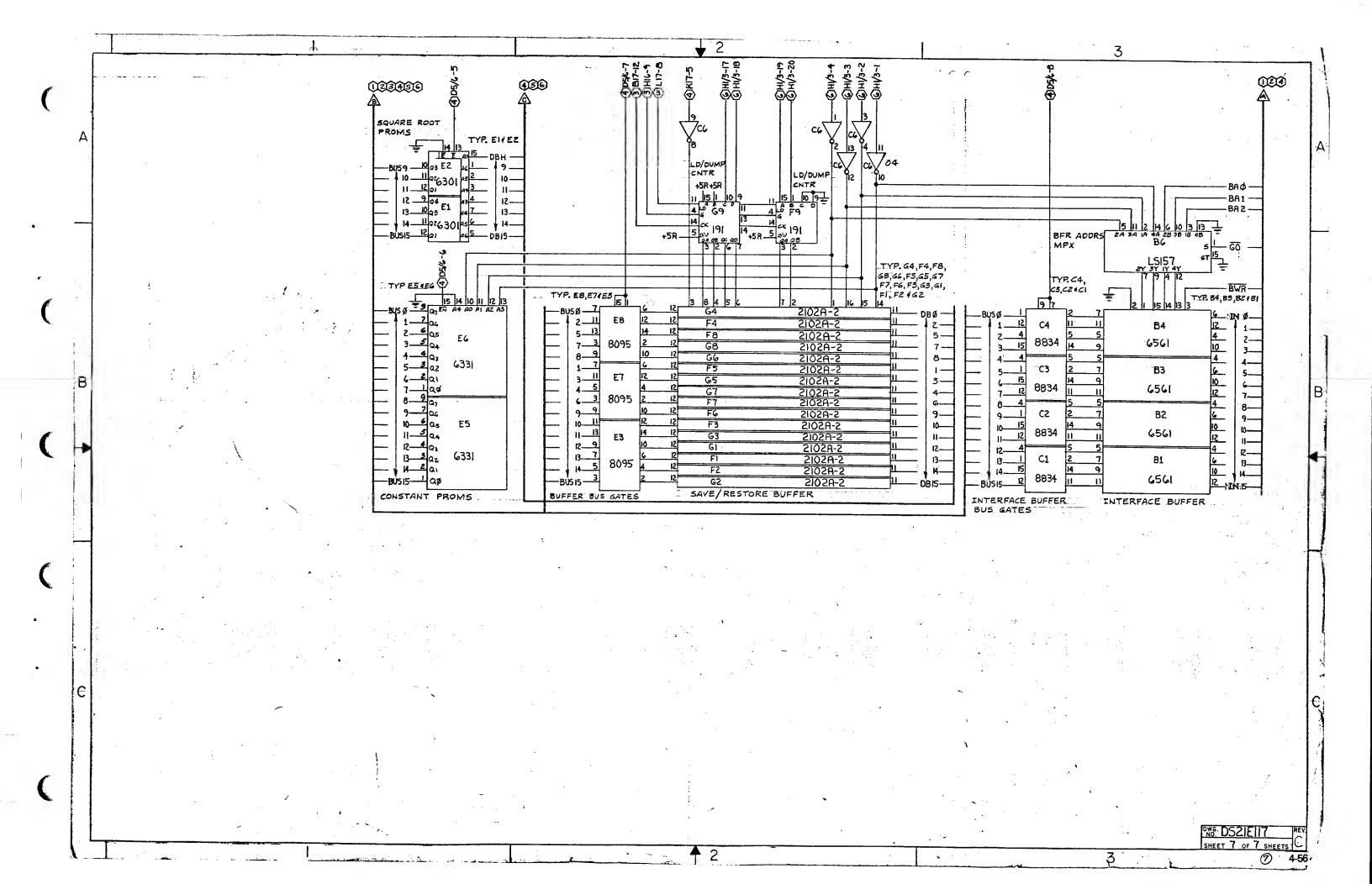












128/32K A/B-Port Memory Unit

4-57
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0A21E250-X CONFIGURATION TABLE

		SINGLE PORT	OUAL PORT. DISTRIBUTED MODE	DUAL PORT. QPU MDDE	SINGLE PORT 32K
4K	PDPULATED WITH RAMS (MK 4027-3)	USE CONFIGURATION BLOCKS A.AL.B	USE CONFIGURATION BLOCKS A.AL.C.D.E	USE CONFIGURATION BLOCKS A.C.O.E	
18	POPULATED WITH (RAMS (MK 4216-3)	DA21E250-02 USE CONFIGURATION BLOCKS B.F	OA21E26D-01 USE CONFIGURATION BLOCKS D.E.F.Q	DA21E250-01 USE CONFIGURATION BLOCKS E.F.H	DA21E250-D3 USE CONFIGURATION BLOCKS ALI

CONFIGURATION BLOCK A) 32K HARDWARE CONFIGURATION (USING 4K RAMS)

- 1) REMOVE R22
 2) ADJUST POT R31 SUCH THAT TP HAS A 29 JUS REP RATE
 3) INSERT JUMPERS: JP9-2 , JP11-2 , JP13-2
 4) POPULATE MEMORY ARRAY WITH MK4027-3 MEMORY CHIPS

CONFIGURATION BLDCK AD APORT 32K ADDRESSING CHART

*APORT FIELD	AMCO	AMC1	AMC2	AM C3	**CLOSED CONTACTS ON SWITCH PACK IV
0	Н	Н	Н	н	8
1	н	Н	Н	L	7.8
2	н	Н	L	Н	6.6
3	н	Н	L	L	6.7.8
4	Н	L	Н	Н	5.8
5	н	L	Н	L	5.7.8
8	н	L	L	Н	6.8.8
7	н	L	L	L	5.8.7.8
8	L	Н	Н	Н	4.8
8	L	Н	Н	L	4.7.8
10	L	Н	L	Н	4.6.8
11	L	Н	L	L	4.6.7.8
12	L	L	Н	Н	4.5.8
13	L	L	Н	L	4.5.7.8
14	L	L	L	Н	4.5.8.8
15	L	L	L	L	4.5.6.7.8

- * EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
- ** ALL DTHER CONTACTS ON SWITCH PACK 1Y OPEN

CONFIGURATION BLOCK B) SINGLEPORT CONFIGURATION i) DEPOPULATE PC BOARD AS PER BM21E260-02 2) ADD JUMPERS JP3 . JP5 . JP7

CONFIGURATION BLOCK C) BPORT 32K MEMORY ROW SELECT 1) INSERT JUMPERS: JP10-2 . JP12-2 . JP14-2

CONFIGURATION BLOCK O) BPORT 32K ADDRESSING AND I/O DEVICE CODE CHART

*BPORT FIELD OR I/D DEVICE CODE	BMCO DR BDSO	BMCI OR BDSI	BMC2 OR BDS2	DR BDS3	**CLDSED' CONTACTS ON SWITCH PACK 128
0	Н	Н	Н	Н	8
1	Н	Н	Н	L	4.8
2	Н	Н	L	Н	3.8
3	Н	Н	L	L	3.4.8
4	Н	L	Н	Н	2.8
6	Н	L	Н	L	2.4.8
	н	L	L	Н	2.3.8
7	Н	L	L	L	2.3.4.8
8	L	Н	н	Н	1.6
	L	н	н	L	1.4.8
10	L	н	L	Н	1.3.8
11	L	н	L	L	1.3.4.8
12	L	L	Н	Н	1.2.6
13	L	L	Н	L	1 .2 .4 .6
14	L	L	L	Н	1 .2 .3 .6
15	L	L	L	L	1.2.3.4.6

- * EACH FIELD ND. REPRESENTS ONE 32K SEGMENT OF MEMORY
- ** ALL DTHER CONTACTS ON SWITCH PACK 128 AND 9C OPEN

CONFIGURATION BLOCK E) LAST BOARD IN DAISY CHAIN

THE LAST QUAL PORT MEMORY BOARD IN A QAISY CHAIN MUST TERMINATE BPORT BUS SIGNALS. THE LAST DUAL PORT MEMORY IN A DAISY CHAIN DNLY MUST HAVE THE FOLLOWING RESISTORS: RP8.RP7.RP8. RP12 , RES PACK 12F

CONFIGURATION BLOCK F) 128K HAROWARE CONFIGURATION/APDRT 128K ADDRESSING M

- 1) R2O ANO R22 INSERTED
- 1) RZO ANO RZZ INSERTED
 2) INSERT JIMPER JP4
 3) ADJUST POT R31 SUCH THAT TP HAS A 14.5 JS REP RATE
 4) INSERT JUMPERS JP9 . JP11 . JP13
 5) POPULATE MEMDRY ARRAY WITH MK4118-3 MEMDRY CHIPS
 8) APORT 128K ADDRESSING CHART

*APDRT FIELD NO.	AMCD	AMC1	AMCZ	AMC3	AMC3	**CLOSEO CONTACTS ON SWITCH PACK 1V
0.1.2.3	Н	Н	н	Н	н	
4.5.8.7	Н	Н	н	Н	L	6
8,9,10,11	Н	Н	н	L	Н	4
12,13,14,15	Н	Н	Н	L	L	4.5
18.17.18.19	н	Н	L	Н	Н	3
20.21,22,23	н	Н	L	Н	L	3.5
24.25.28.27	н	н	L	L	Н	3.4
28.29.3D.31	Н	Н	L	L	L	3.4.5
32, 33, 34, 35	н	L	Н	Н	н	2
38, 37, 38, 39	Н	L	Н	Н	L	2.5
40.41.42.43	Н	L	н	L	Н	2.4
44.45.48.47	Н	L	Н	L	L	2.4.5
46.49.5D.51	н	L	L	Н	Н	2.3
62.63.64.66	н	L	L	Н	L	2.3.5
56,57,58,59	Н	L	L	L	Н	2.3.4
80.61,62.83	н	L	L	L	L	2.3.4.5
64,65,66,67	L	Н	н	Н	Н	1
68,69,70,71	L	Н	Н	Н	L	1.5
72.73.74.75	L	Н	н	L	Н	1.4
76,77,78,78	L	Н	Н	L	L	1.4.5
80.81,82.83	L	Н	L	н	Н	1.3
84.85.86.67	L	Н	L	Н	L	1.2.5
88.89,90,91	L	Н	L	L	Н	1.3.4
92.93.94.95	L	Н	L	L	L	1.3.4.5
98,97,98,99	L	L	Н	Н	Н	1.2
100.101.102.103	L	L	Н	Н	L	1.2.5
104.105.106.107	L	L	Н	L	Н	1.2.4
106.109.110.111	L	L	Н	L	L	1.2.4.5
112.113.114.115	L	L	L	Н	Н	1.2.3
118.117.116.119	L	L	L	Н	L	1.2.3.5
120.121.122.123	L	L	L	L	Н	1.2.3.4
124,125,126,127	L	L	L	L	L	1.2.3.4.5

- * EACH FIELD NO. REPRESENTS ONE 32K SEGMENT DF MEMORY (TO EXPAND BEYOND 15 FIELDS . IC 2X AND 2Y . SHT.7 . MUST BE ADDED)
- ** ALL DTHER SWITCH CONTACTS ON SWITCH IV ARE OPEN

CONFIGURATION BLOCK Q) 125K APORT/32K BPORT COMMON MEMORY WITH JUMPERS JP10. JP12. JP14. INSERTED

BMC2	BMC3	COMMON SEGMENT OF APORT 128K MEMORY
Н	Н	1ST 32K
Н	L	2NO 32K
L	Н	3RO 32K
L	L	4TH 32K

2) TO FORCE COMMON APORT/BPORT MEMORY INDEPENDENT OF BMC2 AND BMC3

BMC2	BMC3	COMMON SEGMENT OF APORT 128K MEMORY	JUMPERS INSERTED
X	X	15T 32K	JP1D. JP15. JP18
X	X	SND 35K	JP10. JP18
X	X	3RD 32K	JP10. JP15
X	X	4TH 32K	JP10

WHERE X - DONT CARE

CONFIGURATION BLOCK H) BPDRT 128K ADDRESSING CONFIGURATION

- 1) INSERT JUMPERS JP10. JP12, JP14
- 2) BPDRT 128K ADDRESSING CHART

BPDRT FIELD NO.	BMAGO	BM AD1	BMAD2	BMCO	BMC1	**CLOSED CONTACTS ON SWITCH PACKS			
						9C	128		
0.1.2.3	н	H	Н	Н	Н		8		
4.5.8.7	н	н	н	Н	L		2.8		
8,9,10,11	н	Н	Н	L	Н		1.8		
12,13,14,15	н	н	н	L	L		1,2.6		
18.17.18.19	н	Н	L	Н	н	7	8		
20,21,22,23	н	Н	L	Н	L	7	2.8		
24.25.2B.27	Н	Н	L	L	Н	7	1.6		
26.29.30.31	н	Н	L	L	L	7	1.2.6		
32.33.34.35	Н	L	Н	Н	Н	6	8		
38,37,38,39	Н	L	Н	Н	L	6	2.8		
40,41,42,43	Н	L	Н	L	Н	8	1.8		
44.45,4B,47	Н	L	Н	L	L	6	1,2,8		
48,49,50,51	Н	L	L	Н	н	8.7	8		
62,63,64,66	Н	L	L	Н	L	8.7	2.8		
58,57,58,59	Н	L	L	L.	н	8.7	1.6		
80, 81, B2, 63	Н	L	L	L	L	6.7	1.2.8		
64.65.66.67	L	Н	н	Н	Н	6	6		
68.69,70,71	L	Н	Н	Н	L	Б	2.8		
72.73.74.76	L	н	Н	L	Н	6	1.6		
7B,77,78,79	L	н	Н	L	L	6	1.2.6		
80,81,82,83	L	н	L	Н	Н	6.7	8		
84.85.88.87	L	Н	L	Н	L	6.7	2.8		
88.89.9D.91	L	Н	L	L	Н	5.7	1.6		
92.93.94,95	L	Н	L	L	L	5.7	1.2.8		
98,97,98,99	L	L	Н	Н	Н	6.8	6		
100,101,102,103	L	L	Н	Н	L	5.8	2.8		
104,105,108,107	L	L	Н	L	Н	5.6	1.8		
108,109,110,111	L	L	Н	L	L	6.6	1.2.8		
112,113,114,115	L	L	L	Н	Н	5 . 6 . 7	6		
118, 117, 118, 119	L	L	L	Н	L	5.8.7	2.6		
120,121,122,123	L	L	L	L	Н	6.6.7	1.8		
124,125,128,127	L	L	L	L	L	5.8.7	1.2.8		

EACH FIELD NO. REPRESENTS ONE 32K SEGMENT DF MEMDRY ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C DPEN (9C-2 MAY BE CLOSEO TO DISABLE APORT)

CONFIGURATION BLOCK 1) 32K SINGLE PORT CONFIGURATION (USING 16K RAMS) 1) DEPOPULATE BOAROS AS PER ASSEMBLY DAZIEZED-03

DS21E252

MISCELLANEOUS JUMPERS

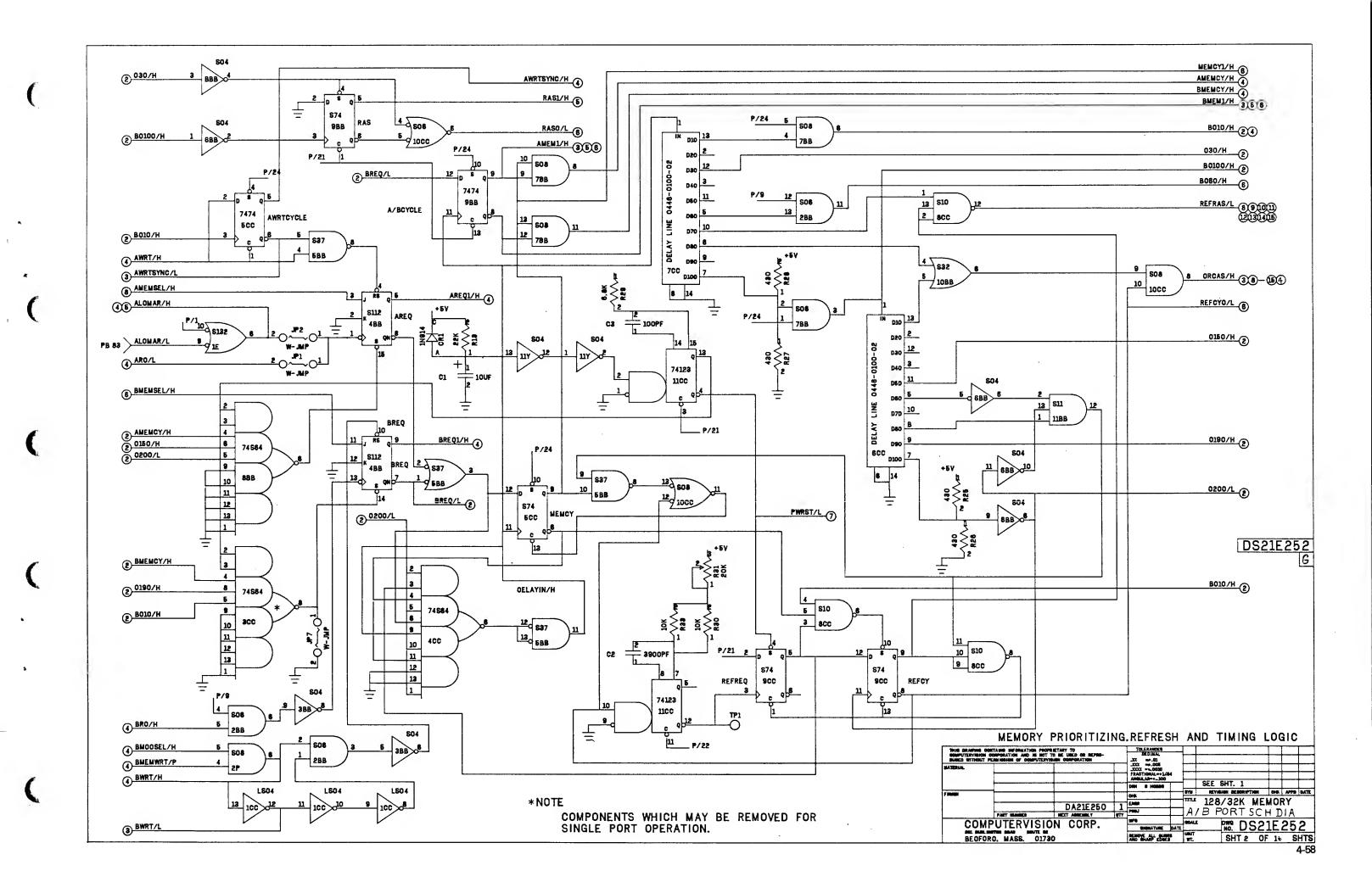
- 1) FOR LOMAR STARTING APORT MEMORY CYCLE INSERT #-2
 2) FOR MEMREAD STARTING APORT MEMORY CYCLE INSERT #-1
 3) FOR GPU MODE REQUIRING DISABLED APORT .
 CLOSE SWITCH 9C-2
- 4) APORT MUC/NON MUC OPERATION

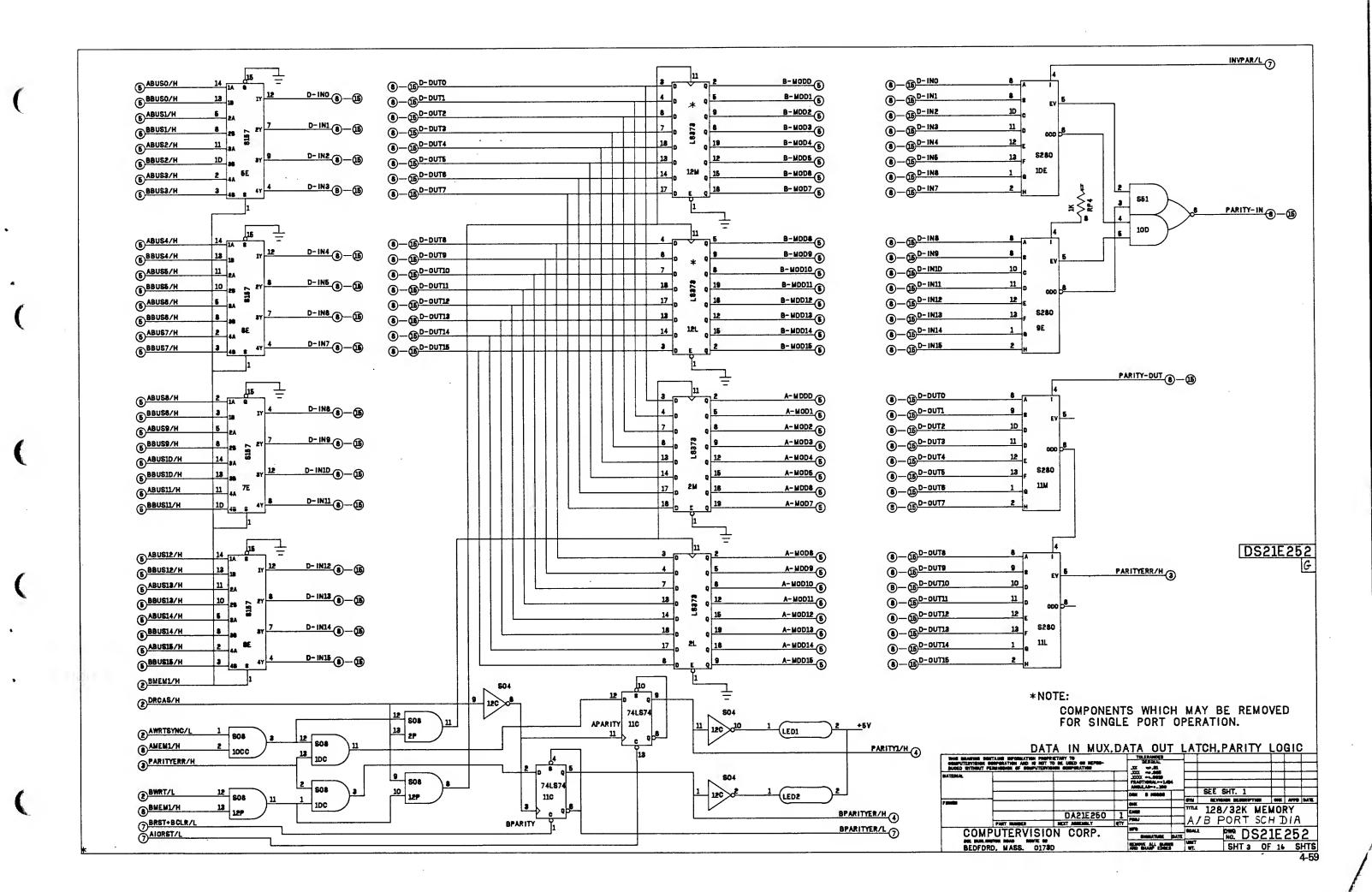
JUMPER PLUG 4D									
MUC	OPERATION	1-18 2-15 3-14 4-13							
NON	MUC OPERATION	5-12 6-11 7-10 8-8							

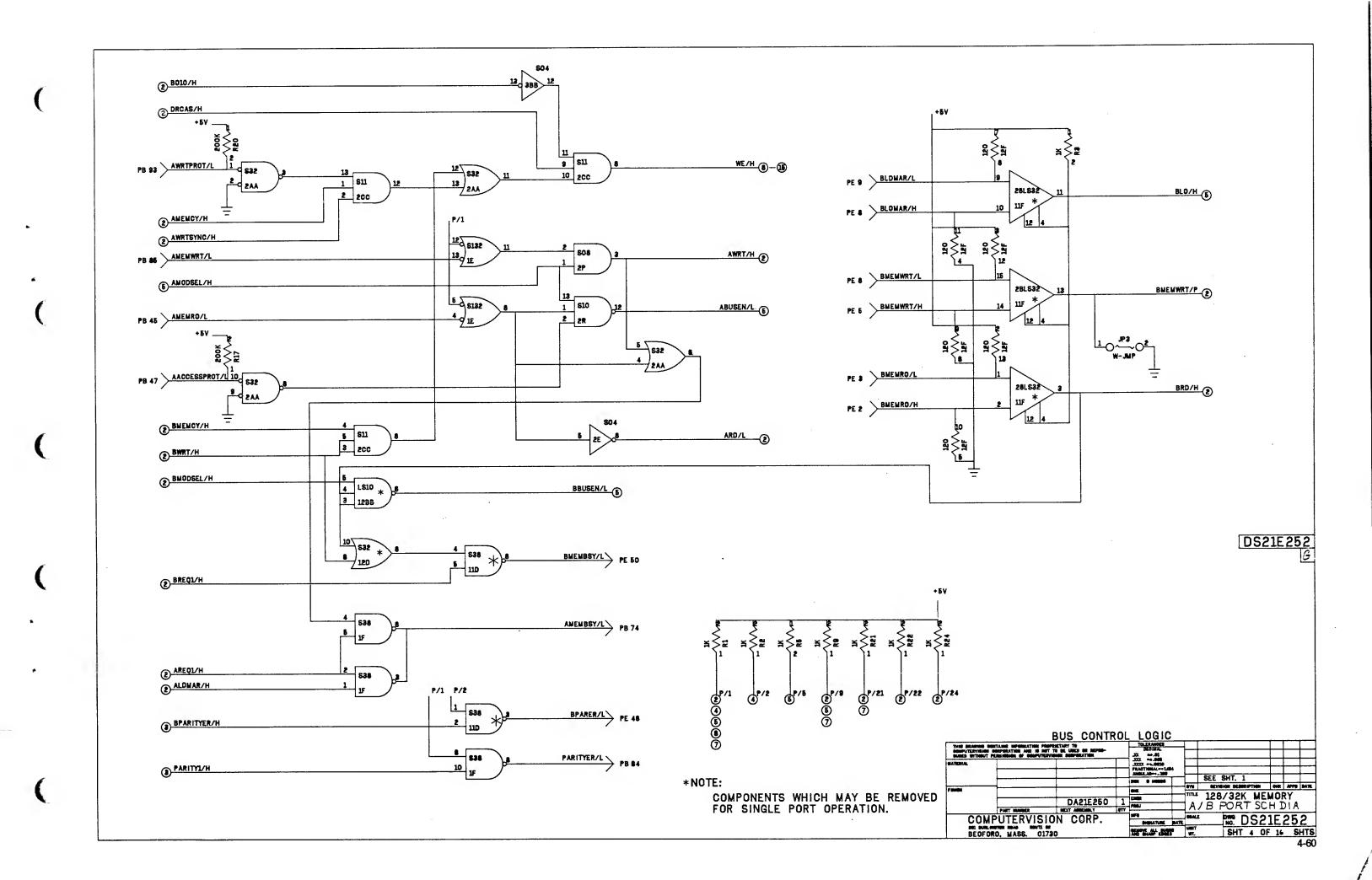
6) APDRT I/O DEVICE CODE

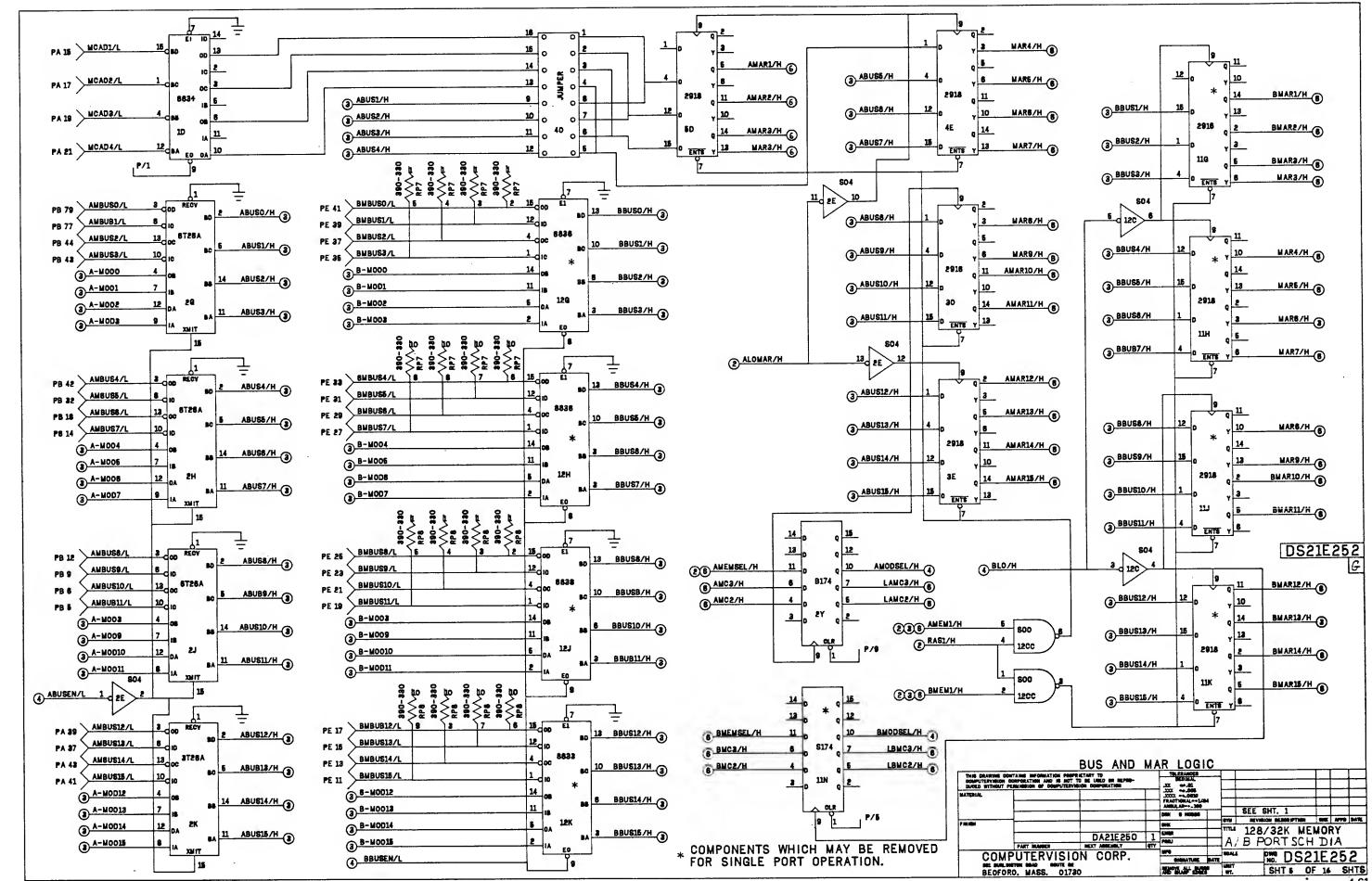
1) STANOARO 24g. INSERT JPS FOR 25g

	STANS DESIGNATION PROPER	TARY TO BE METER-		TOLERANCES DECIMAL	_								17
	MANUTERVIONAN GONFORATION AND 16 NOT 70 ML LIGED OR REPRO- MAKES INTRONT PERMINENER OF BOMPUTERVIONAN GOOPERATION			.D		G	ECO	41	49		70	77./×	1 8/8
MATERIAL.				~		F	ECO	40	916		13	, 20	4/9
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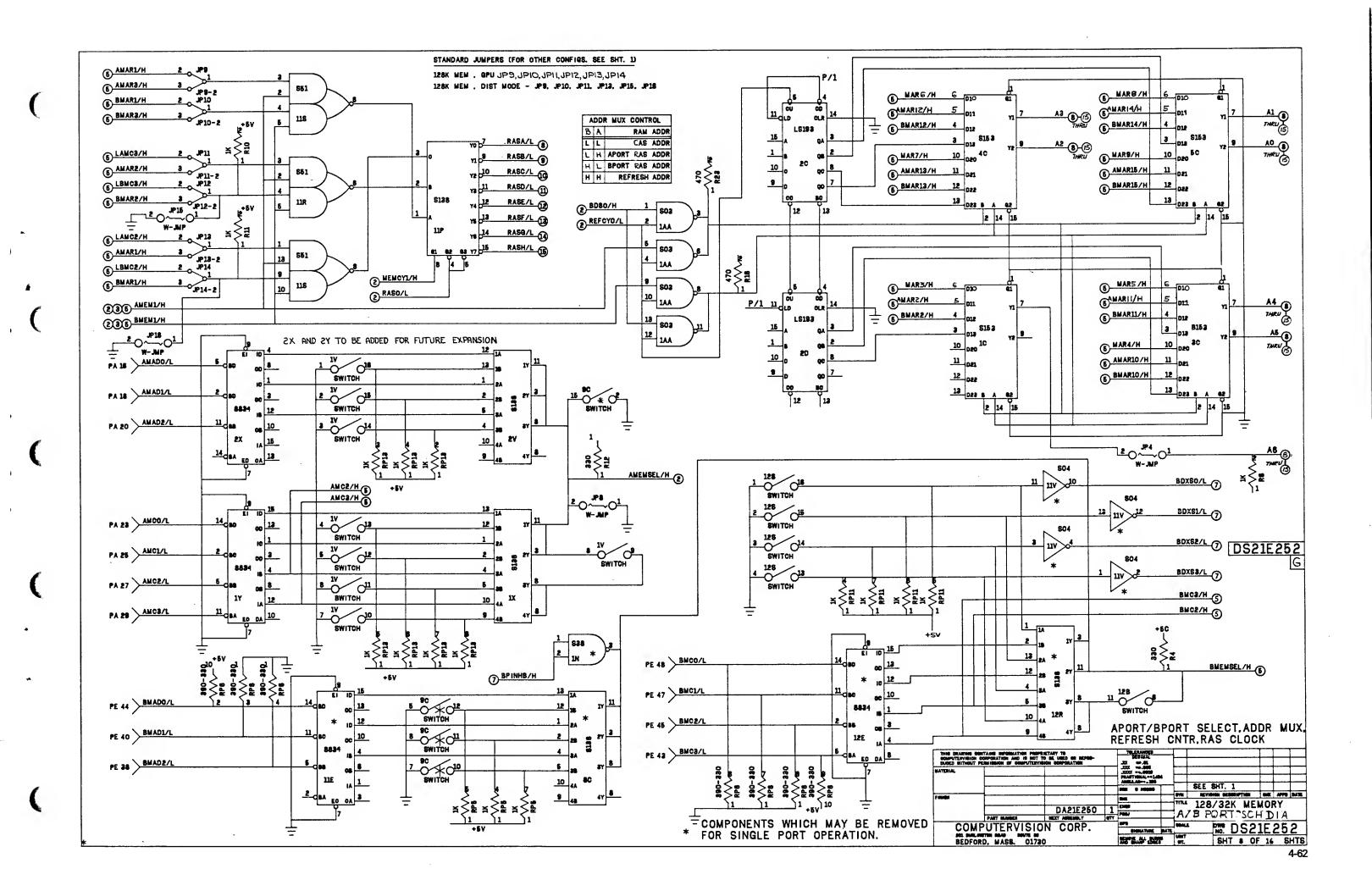


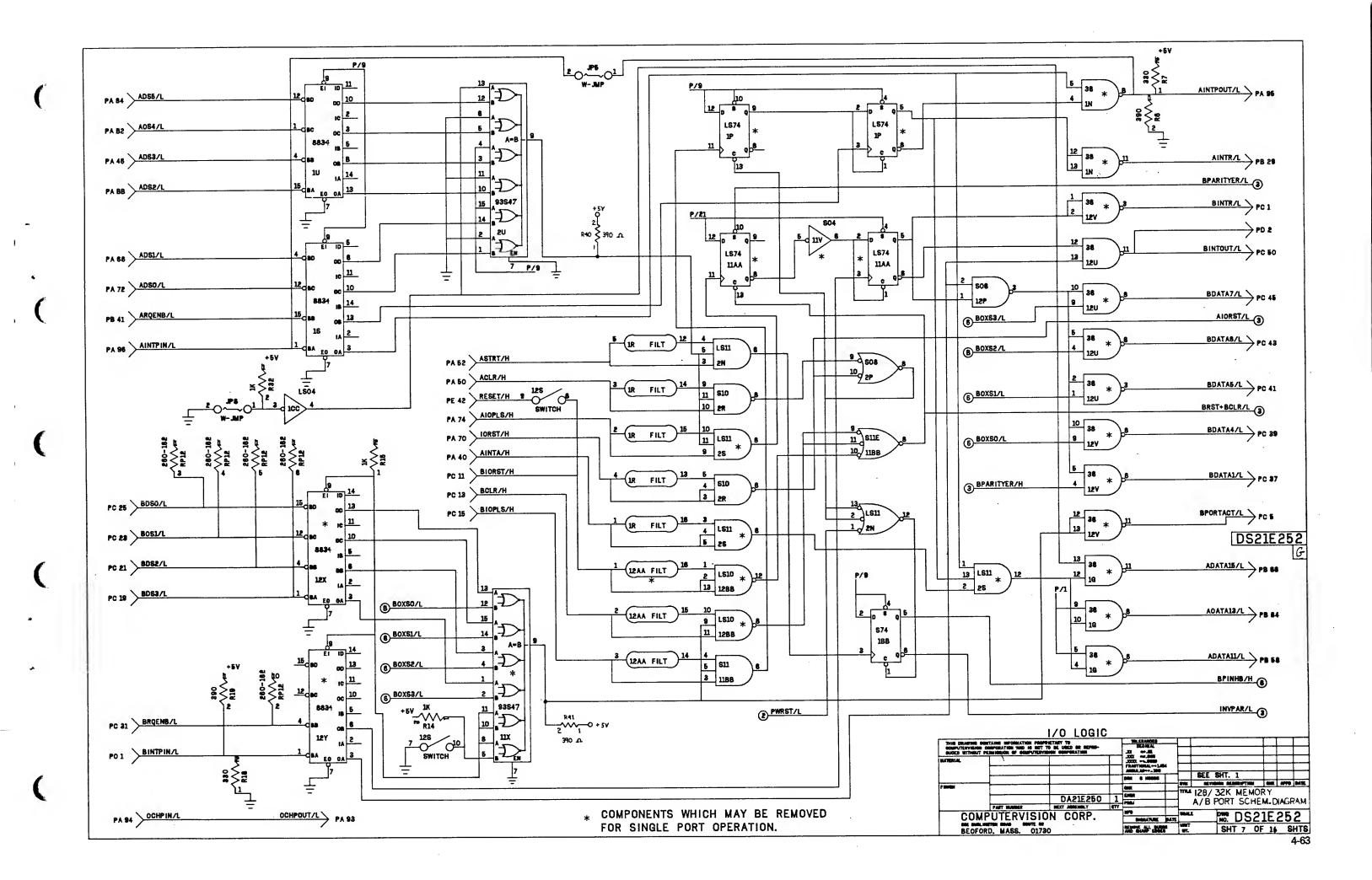


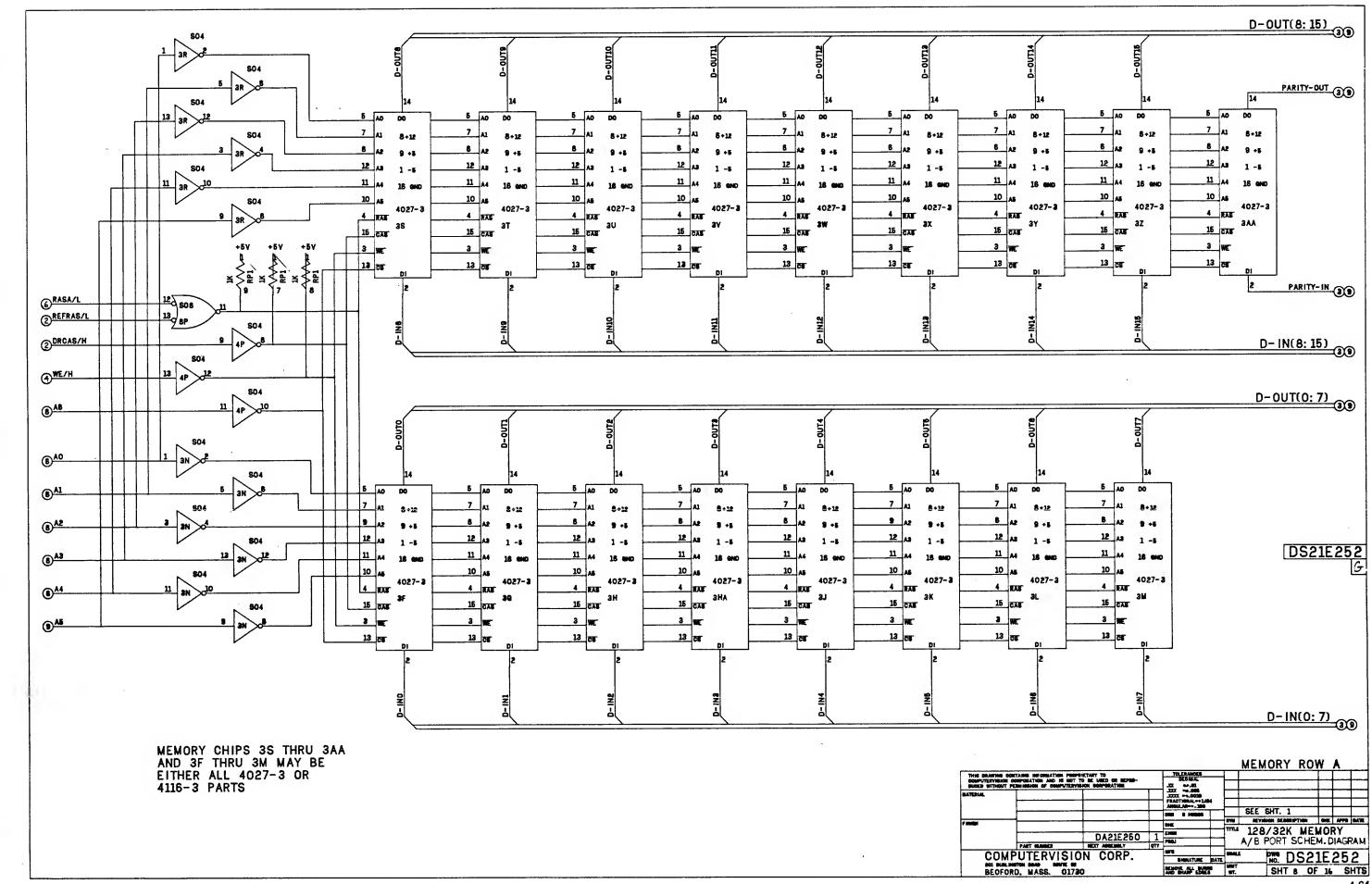


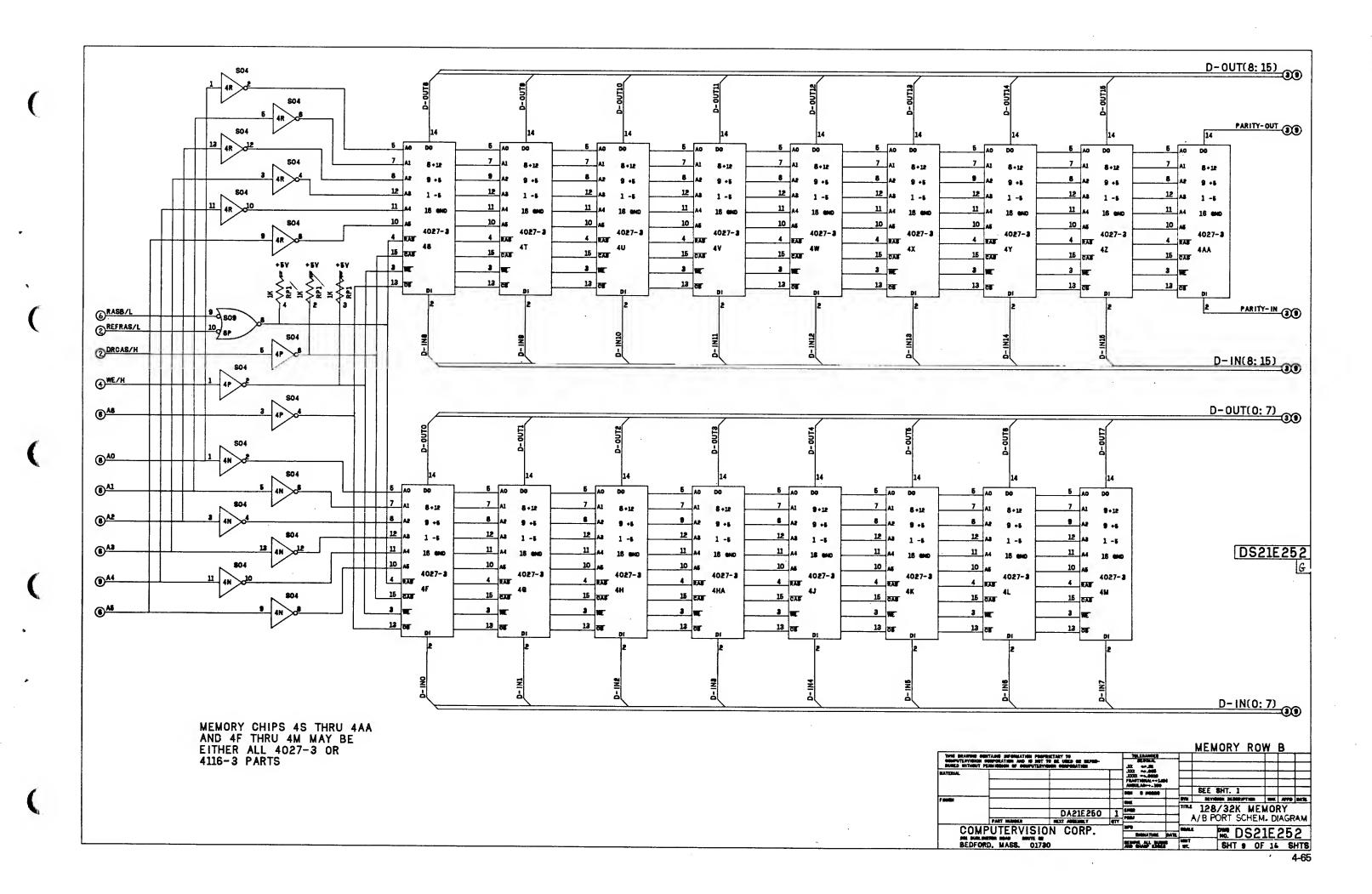


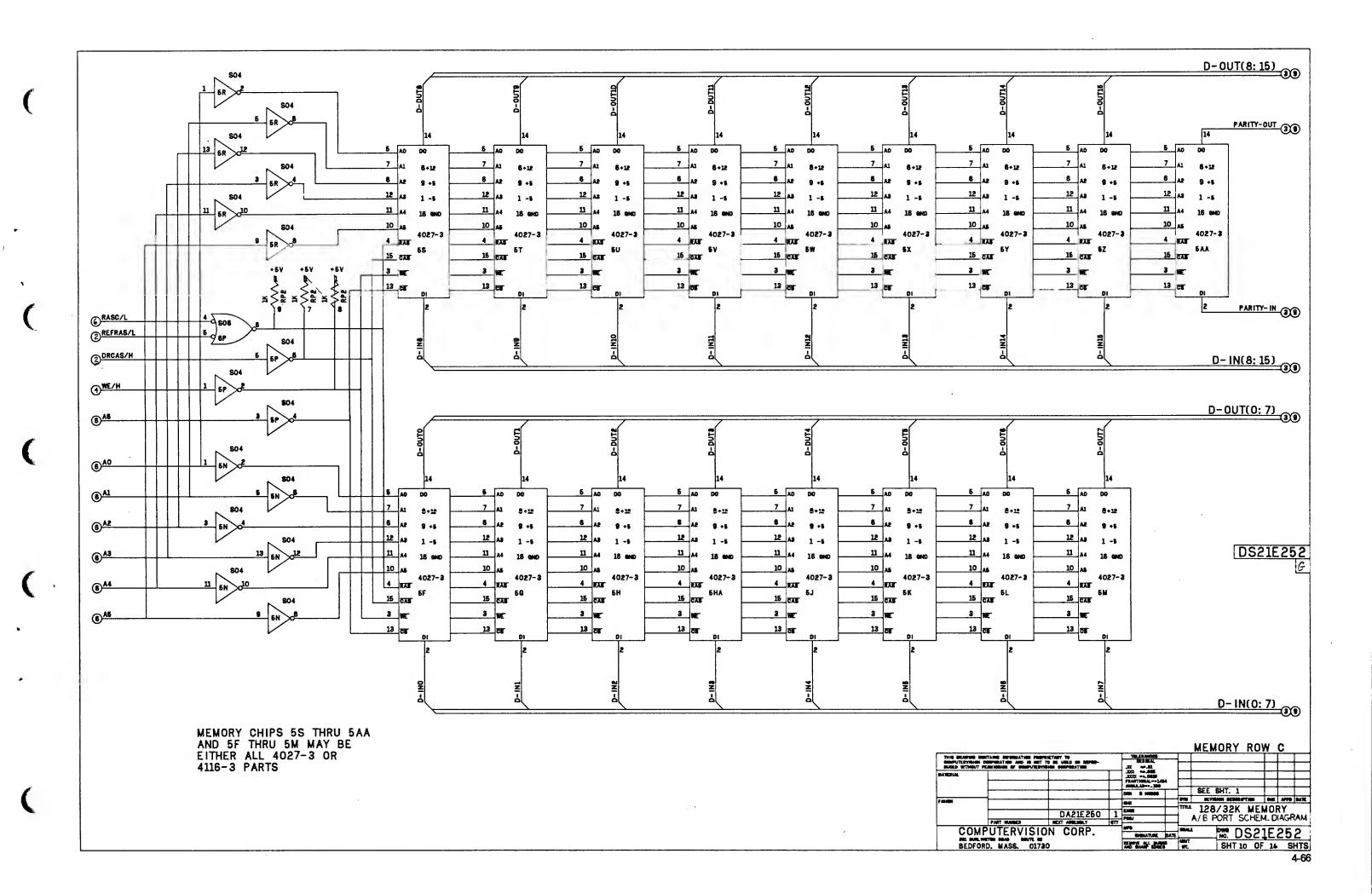
1-61

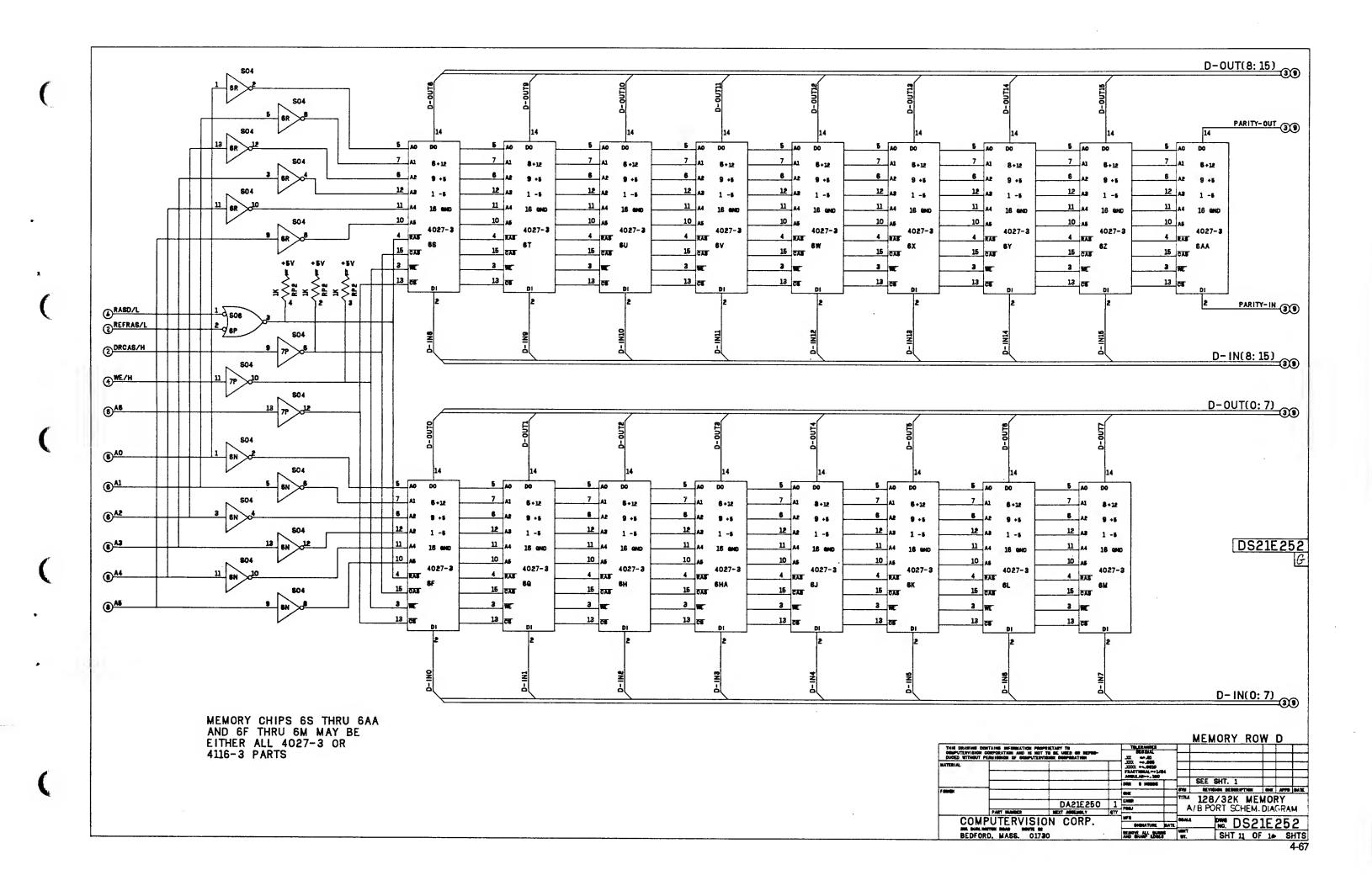


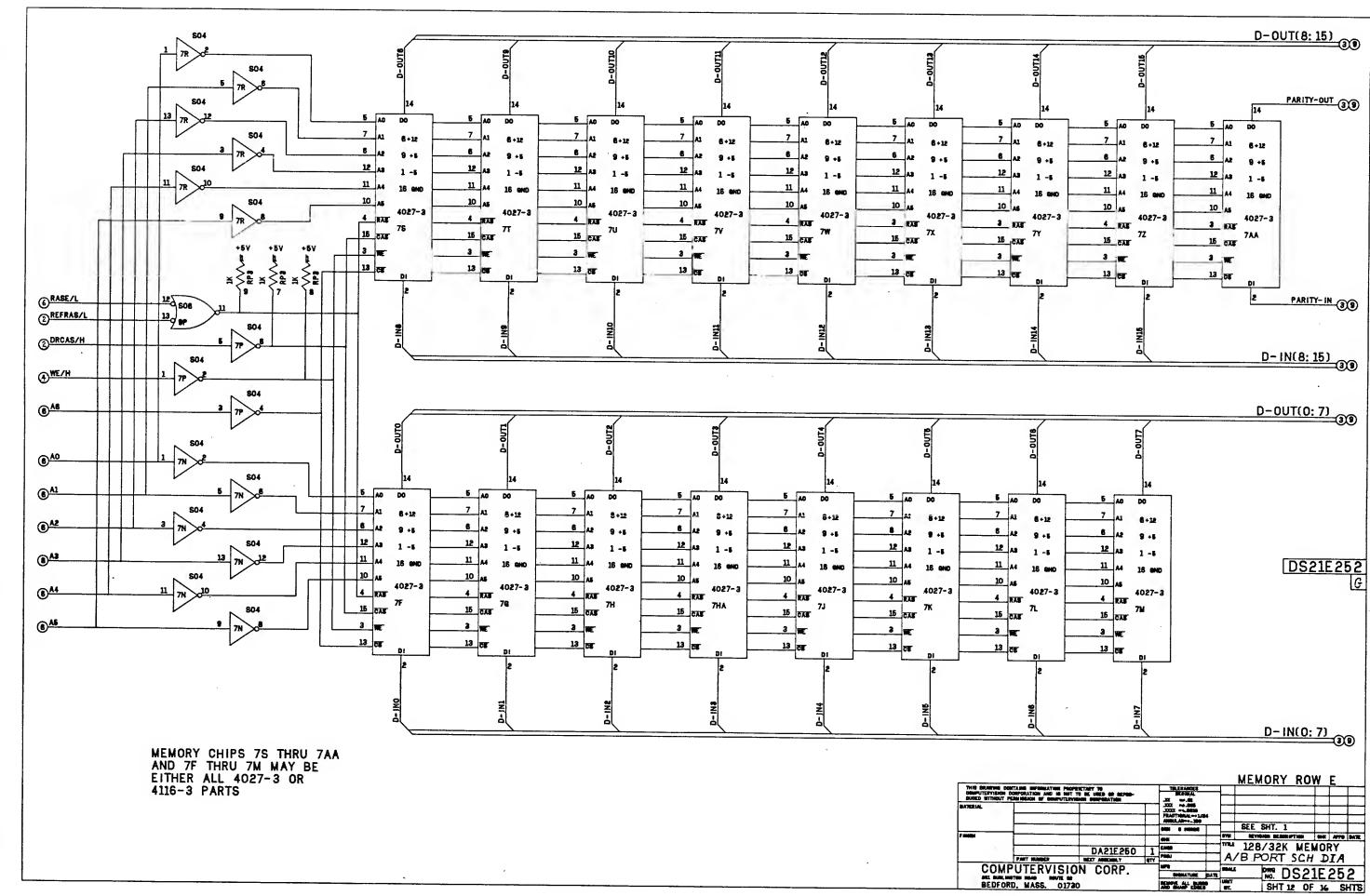


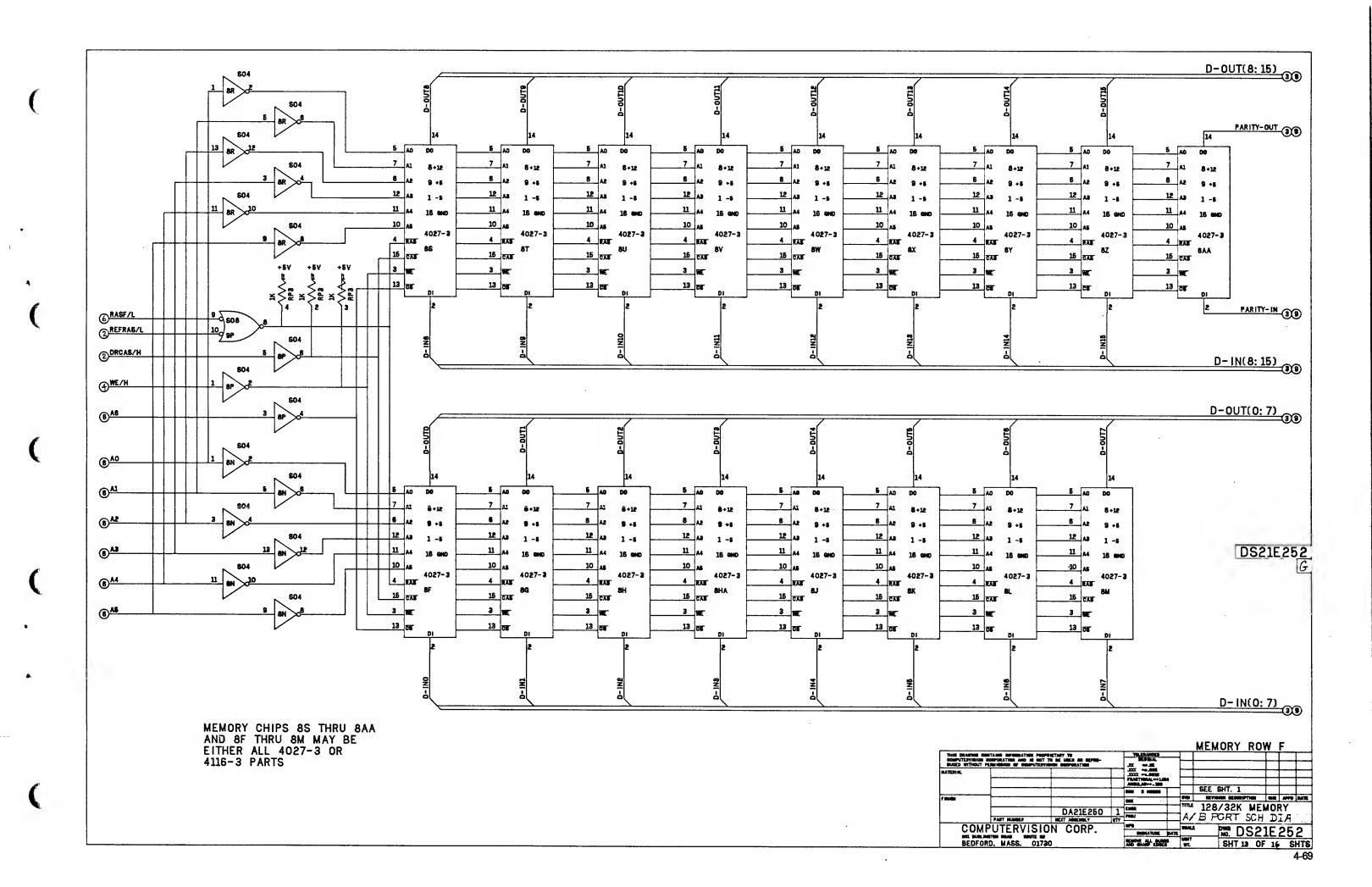


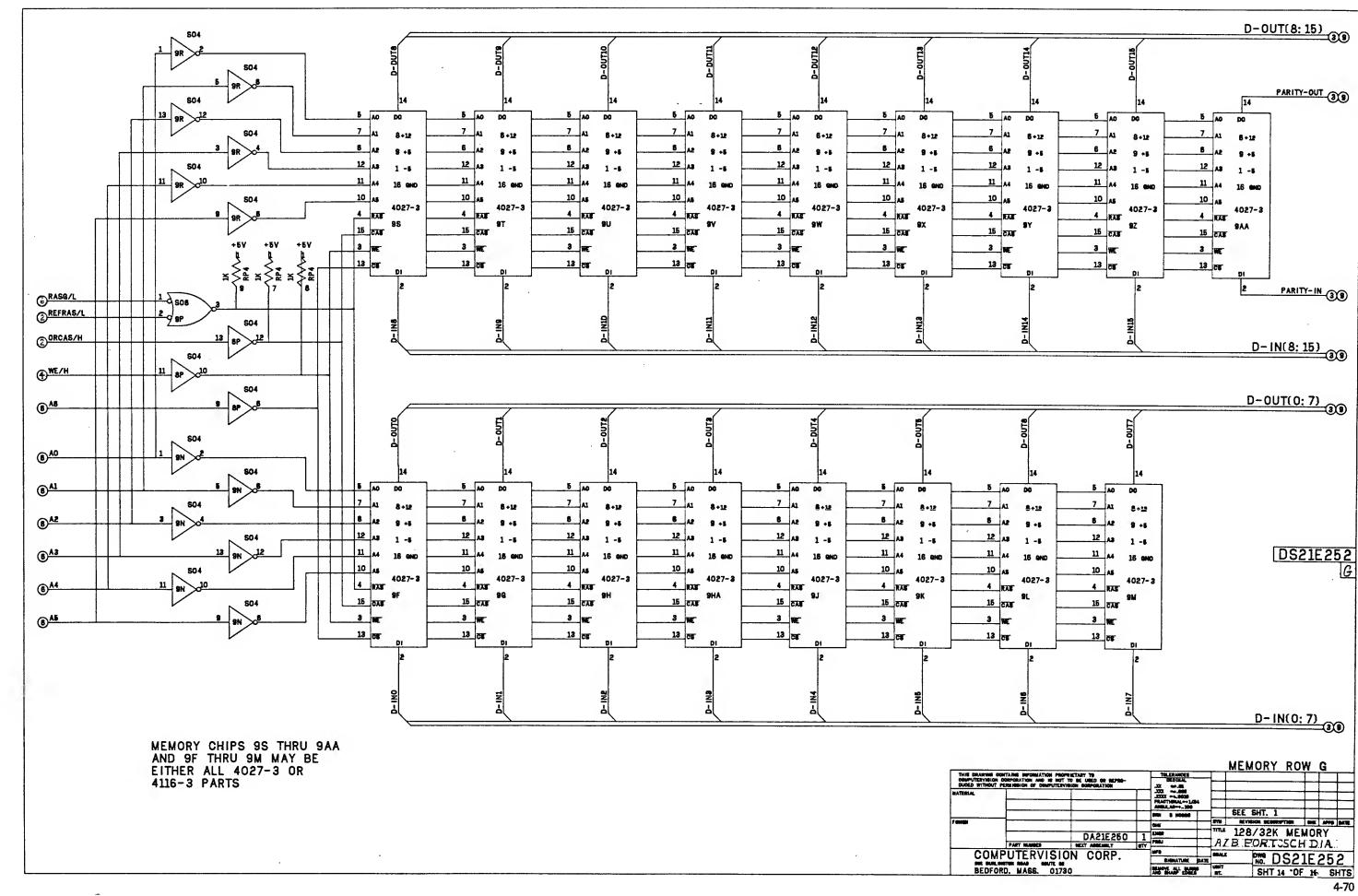




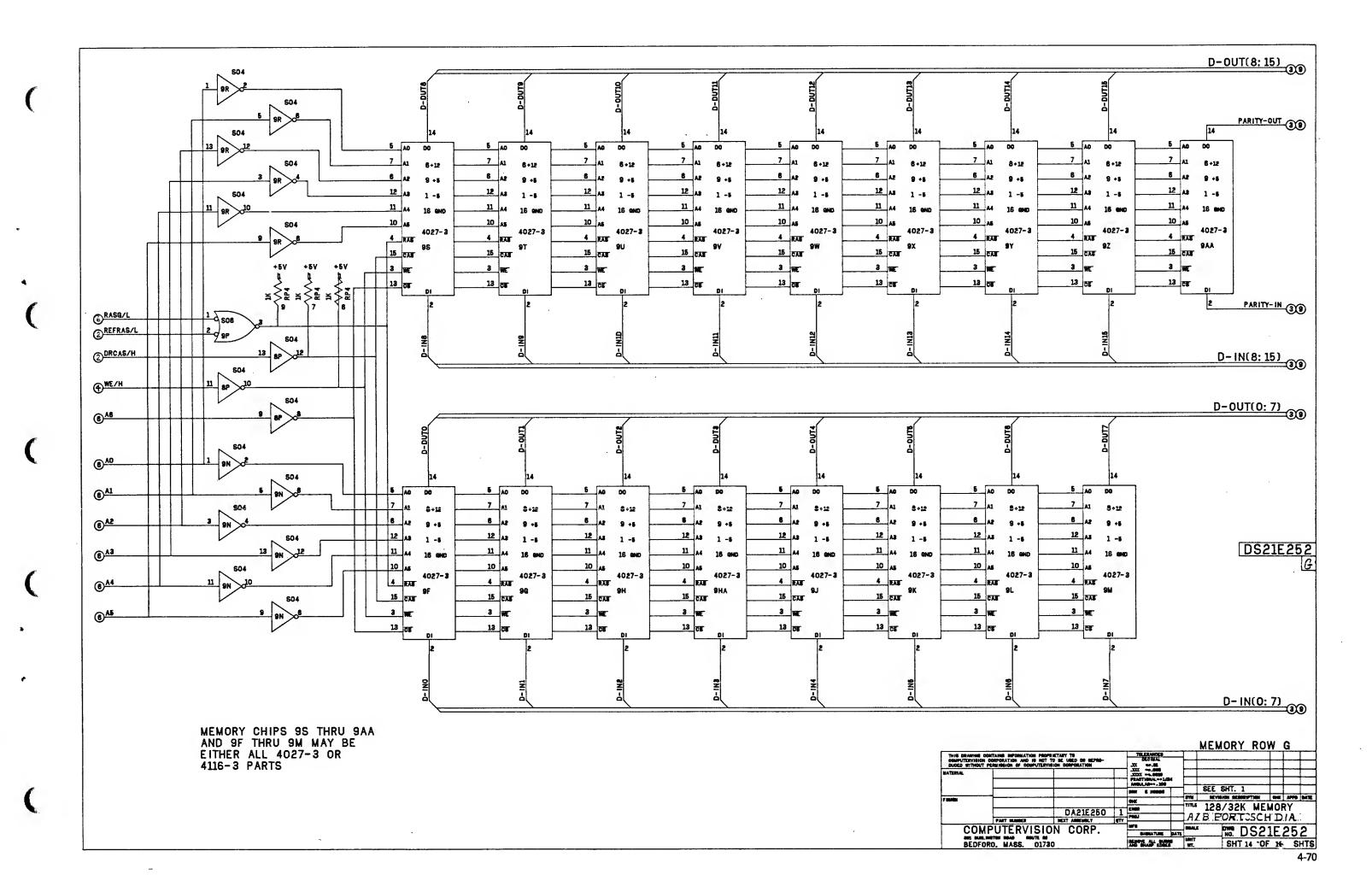


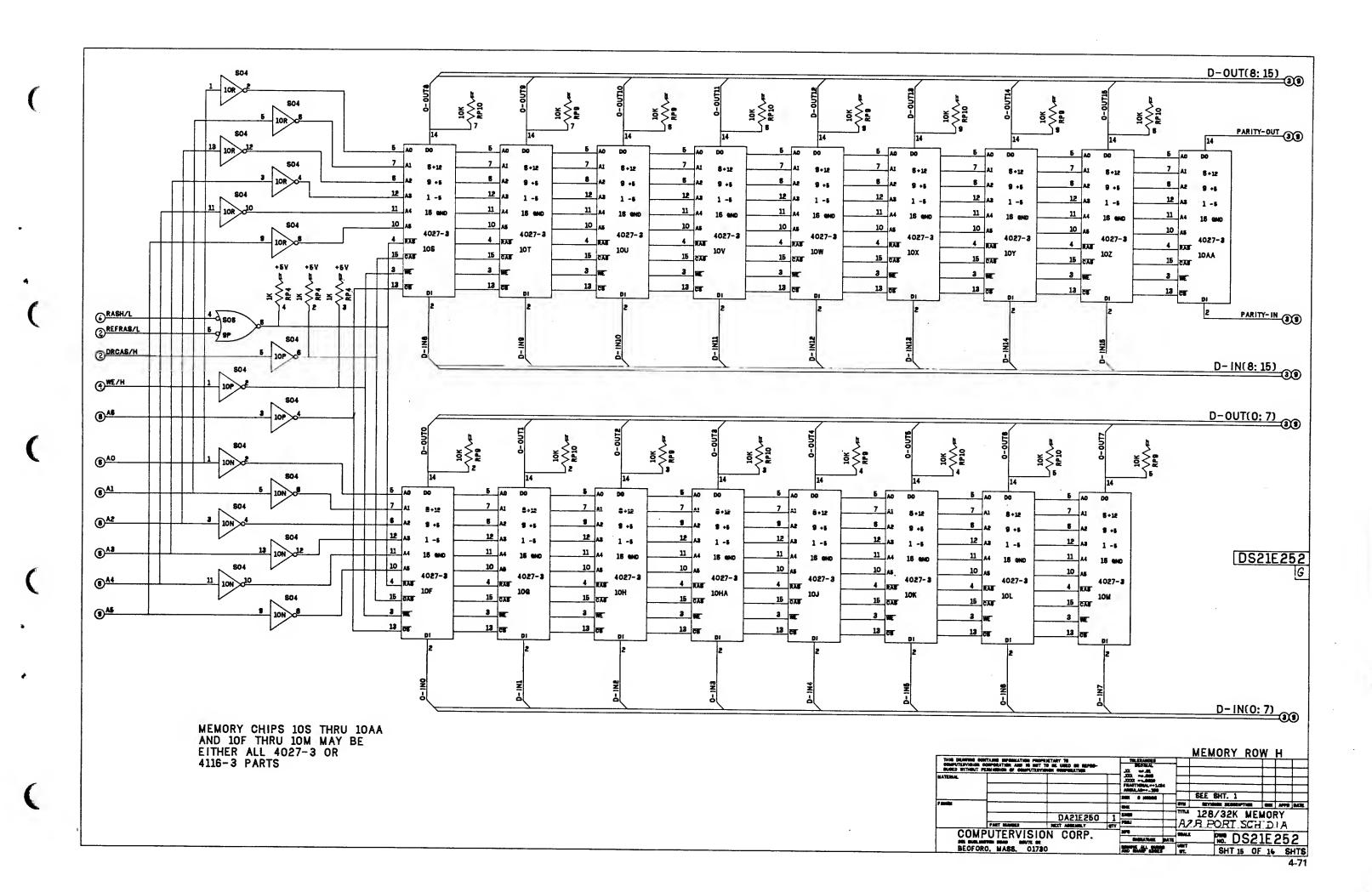






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B PORT CONNECTORS

CONN C

CONN E

BINTR		2
	1	4
BPORTACT		
		8
		10
BIORST		12
BCLR		14
BIOPLS		18
		18
BDS 3		20
BDS 2		22
BDS 1		24
BDS 0		26
		28
		30
BROENB		32
		34
BDATA 10		38
BDATA 1		38
BDATA 4		40
BDATA 5		42
BDATA 5		44
BDATA 7		46
FREE		48
	BINTPOUT	50

			_
1		B MEM RD	2
3	B MEM RD		4
6	B MEMWRY	BMEMWRT	6
7		BLDMAR	8
9	BLOMAR		10
11	8 MEM BUS 18		12
13	B MEM BUS 14		14
15	B MEM BUS 13		16
17	B MEM BUS 12		18
19	B MEM BUS 11		20
21	B MEM BUS 10		22
23	B MEM BUS 9		24
26	B MEM BUS &		26
27	B MEM BUS 7		28
29	B MEM BUS &		30
31	B MEM BUS B		32
33	B MEM BUS 4		34
36	B WEM BUS 3		36
37	B MEM BUS 2	BMAD2	38
39	B MEM BUS 1	BMAD1	40
41	B MEM BUS O	RESET	42
43	BMC 3	BMADO	44
45	BMC 2	BMCO	48
47	BMC I	BPARER	48
49		B MEM BUSY	50
			_

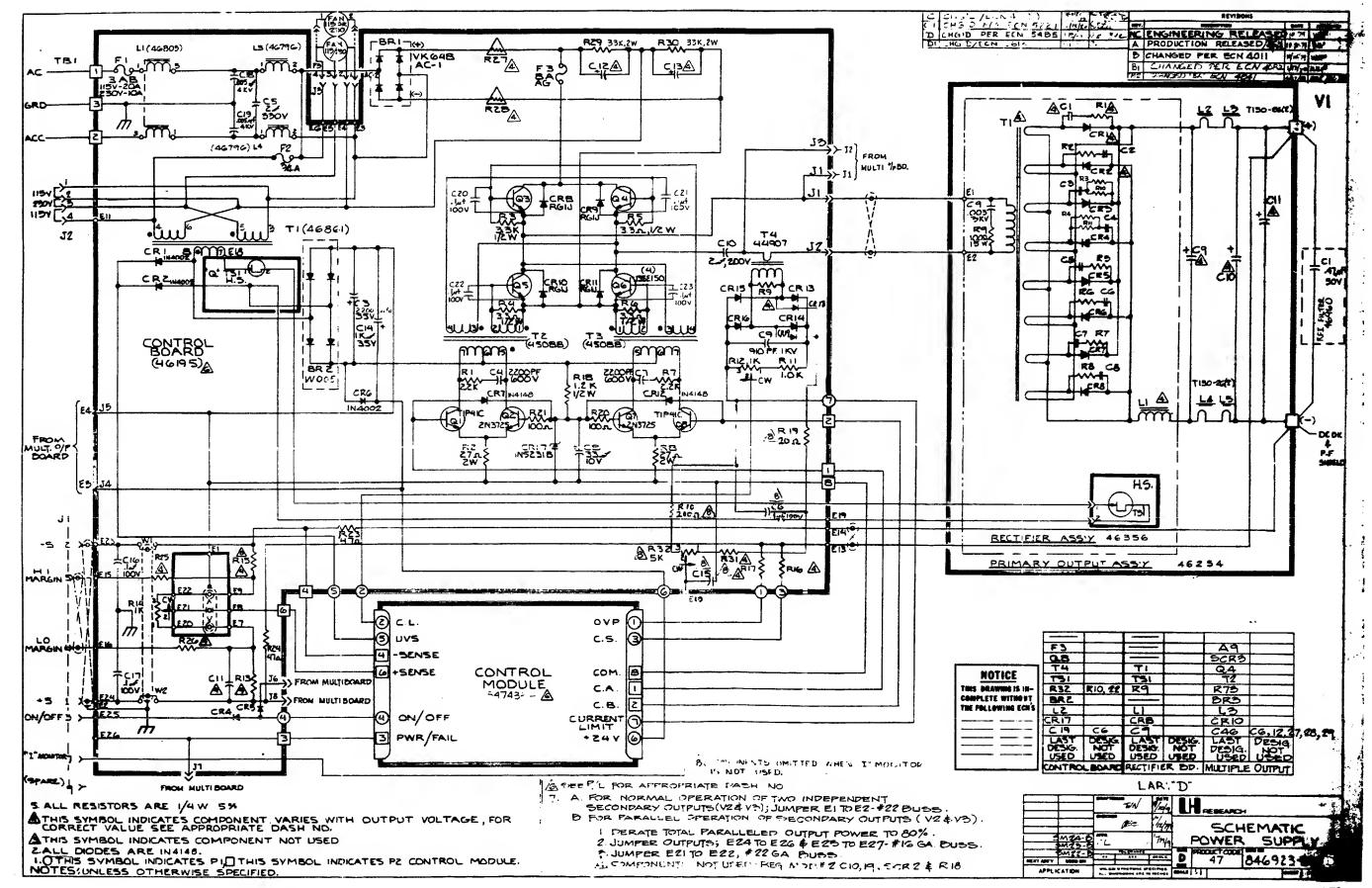
ALL UNUSED PINS GROUNGED

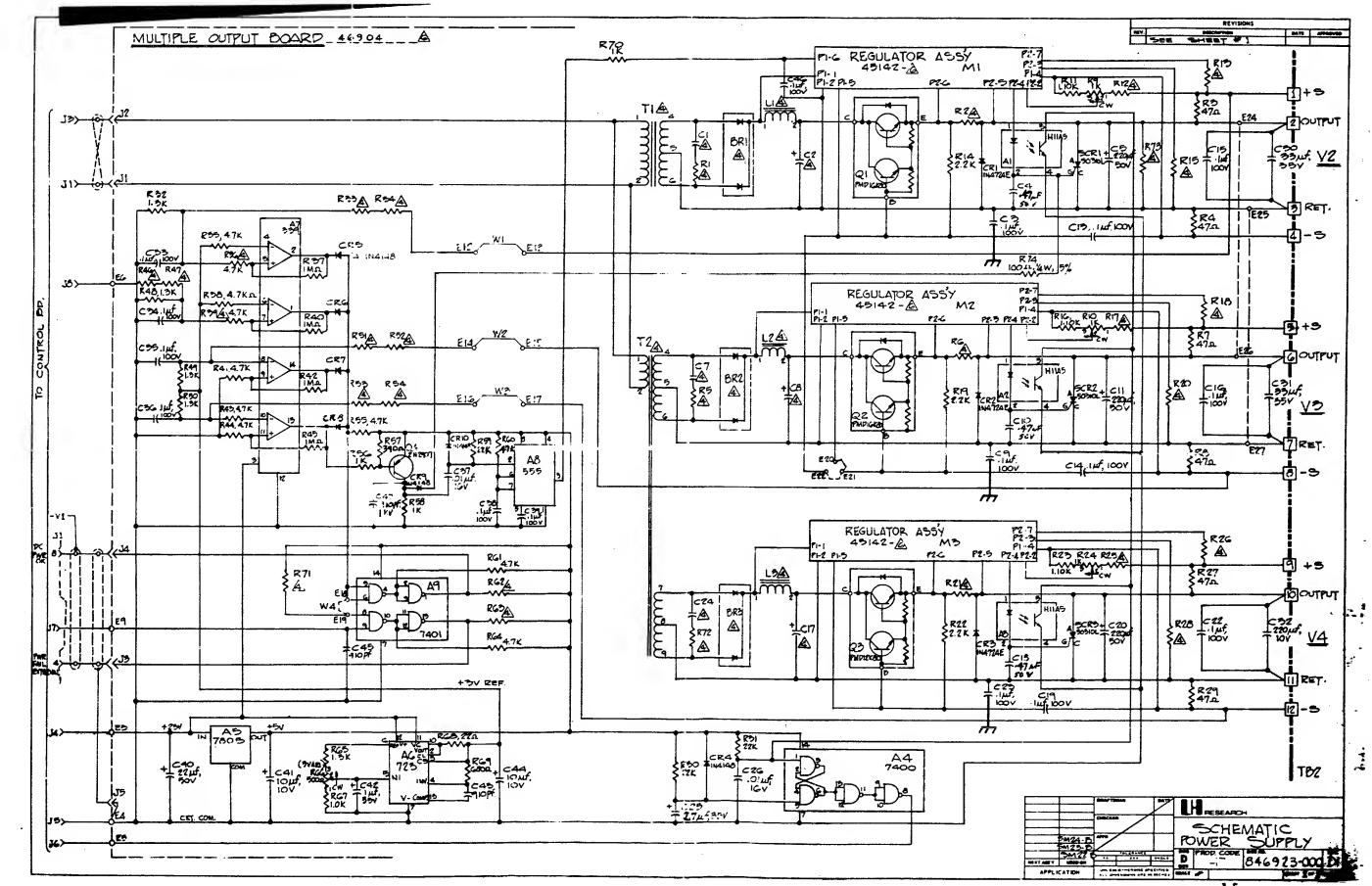
DS21E252

VOLTAGE FEED	S FOR CONNECTORS PA.PB
+12 VOLTS	B48, A7, A8
-6 VOLTS	B81
-12 VOLTS	B71.B72
+5 VOLTS	A/B3,A/B4,A/B97,A/B98
OND	A /P1 A /P2 A /P20 A /P100

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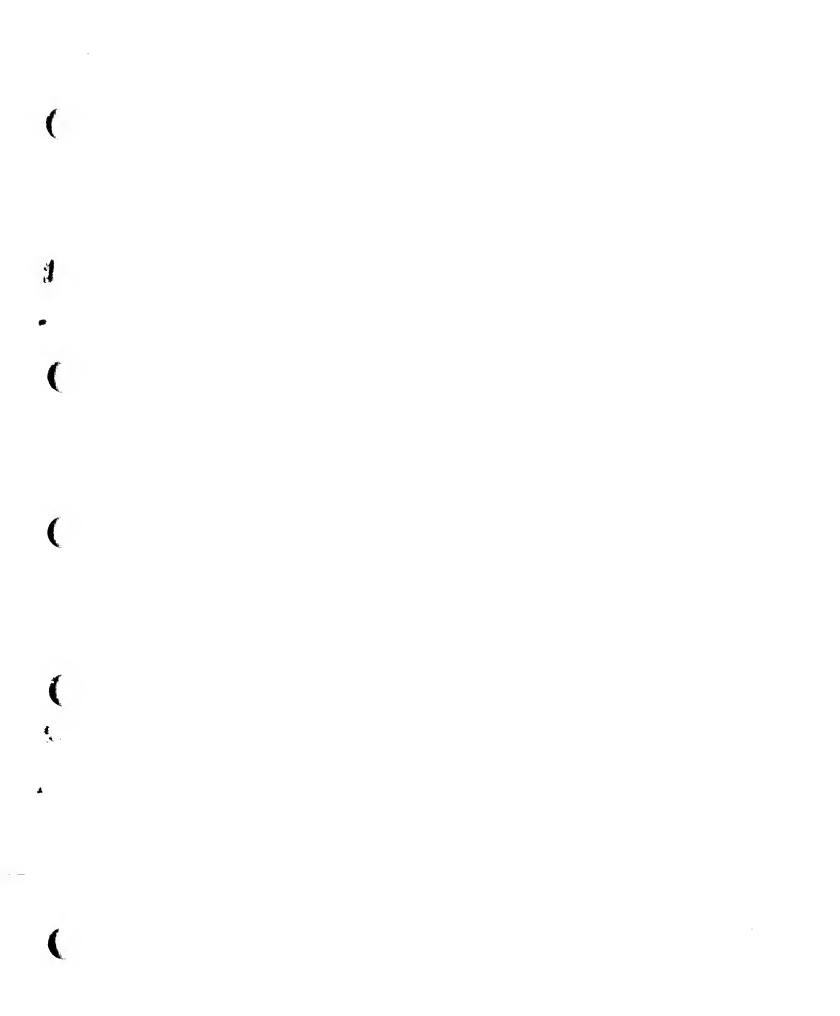
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